XA-AWG

PCI Express XMC Module with Eight 250 MSPS DACs and Artix-7 FPGA V1.1

FEATURES

- Eight 250 MSPS, 16-bit DAC channels
- Up to 74 dB SFDR, 61 dB SNR D/As
- 0.75Vpp AC, 1Vpp DC output range
- x2, x4, x8, x16 Interpolation filters
- DIO on P16 (17 differential pairs)
- Xilinx Artix-7 FPGA
- DDR3 Memory
- Programmable or external sample clock
- Synchronized system sampling using common reference clock and triggers
- Framed, software or external triggering
- Log acquisition timing and events
- Power management features
- PCI Express 2.0 XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, PXIe, or cabled PCI Express application

APPLICATIONS

- Cellular Base Stations
- Diversity Transmit
- Wideband Communications

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL

The XA-AWG is an XMC IO module featuring eight 16-bit, 250 MSPS DAC channels designed for cellular base stations, diversity transmit, and wideband communications.

Flexible trigger methods include counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable PLL clock source.

Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Artix-7 FPGA device. Two 256Mx16 memories provide data buffering and FPGA computing memory.

The Artix-7 FPGA device firmware can be fully customized using VHDL and/or Xilinx System Generator along with the FrameWork Logic toolset

The PCI Express 2.0 interface supports data rates up to 1600 MB/s for unbuffered continuous data or burst data streams. When using a standard configuration involving DDR3 buffered data, a continuous data rate up to 1600 MB/s is supported.

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This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
XA-AWG	80372 80372-0- 80372-1- <ruggedization>	XMC module with eight 250 MSPS DACs, Artix-7 FPGA AC coupled DC coupled <ruggedization>: L1...L4 per Ruggedization Options table
Logic		
FrameWork Logic	55052	XA-AWG FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048G	IO cable with SMA (male) to BNC (female), 1 meter
Options		

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BLOCK DIAGRAM

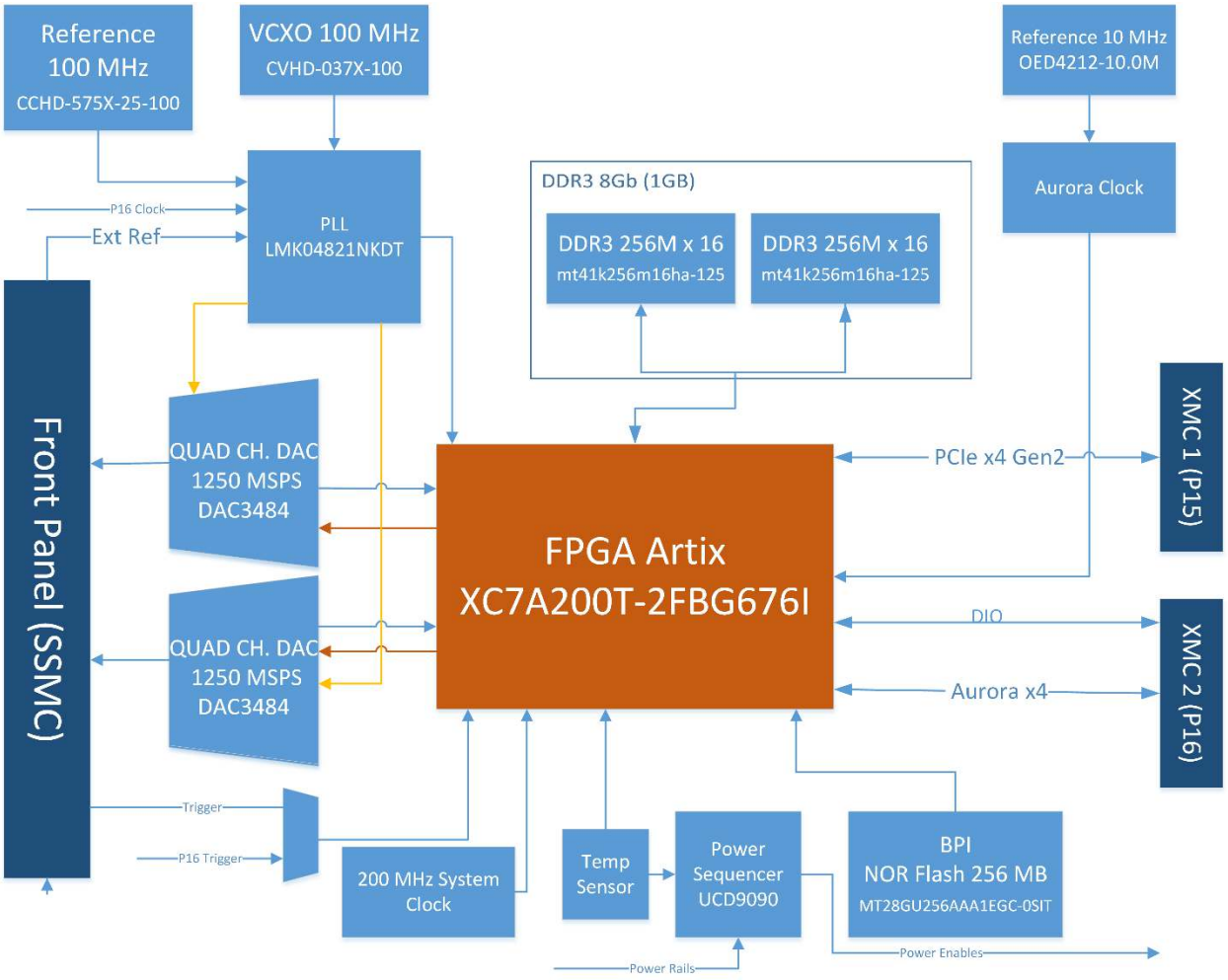

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Illustration 1: Connections available on XA-AWG front panel

XA-AWG

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Standard Features

Analog	
Outputs	8
Output Range	0.75Vpp AC, 1Vpp DC
Output Type	Single ended, AC or DC coupled
Output Impedance	50 Ohm
DAC Device	Texas Instruments DAC3484
DAC Resolution	16-bit
DAC Latency	128 Clock cycles (minimum) with no interpolation
DAC Sample Rate	Up to 250 MHz
Data Format	2's complement, 16-bit integer
Connector	SSMC
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

Memory	
Size	2 devices @ 256Mx16 each
Type	DDR3
Uses	FPGA Buffer Memory FPGA computation memory

Clocks and Triggering	
Clock Sources	Internal 100 MHz 50ppm reference or external
Input Type	Single ended, AC coupled
External Clock Input Range	0.25 – 3.1 Vpp
External Trigger Input Range	1.4 – 2.5 Vpp (centered at 1.25V)
Input Impedance	50 ohm

FPGA	
Logic Cells	215360
Slices	33650
Block RAM	13,140Kb Max
DSP Slices	740
FPGA Device	Xilinx Artix-7 XC7A200T-2FBG676I
Configuration	SelectMAP from PCIe interface JTAG during development
Clock Speed	250 MHz

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Host Interface	
Type	PCI Express 2.0 four lane
Sustained Data Rate	1300 MB/s (DDR3 Max)
Protocol	Packet data
Connector	XMC P15, P16
Interface Standard	PCIe 2.0
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	PLL or External
PLL Output	44 KHz to 2000 MHz
PLL Jitter	< 1 ps RMS
PLL Programming	Host programmed via PCIe
PLL Reference	Internal: 100 MHz clock External reference : J16 input
Triggering	External, software, acquire N frame
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering, clock, and PLL reference are supported.

Acquisition Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked

P16 Digital IO	
Total Number of Bits	34
Balanced Pairs	17
Signal Standard	LVCMOS 2.5V
Drive	±12 mA
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables analog IO power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported.(subset of VITA20)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	TBD
Hazardous Materials	Lead-free and RoHS compliant

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ABSOLUTE MAXIMUM RATINGS Exposure to conditions exceeding these ratings may cause damage!				
Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	0	+3.6	V	
Supply Voltage, VPWR to GND	0	14	V	
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-40	100	C	
ESD Rating	-	2k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS				
Parameter	Min	Typ	Max	Units
Supply Voltage	3.15	+3.3	+3.45	V
Supply Voltage, Nominal 12V VPWR	11.4	12	12.6	V, unless otherwise noted specified and tested with nominal 12V VPWR
DAC Update Rate	0		250	MSPS
Operating Temperature	0		50	C

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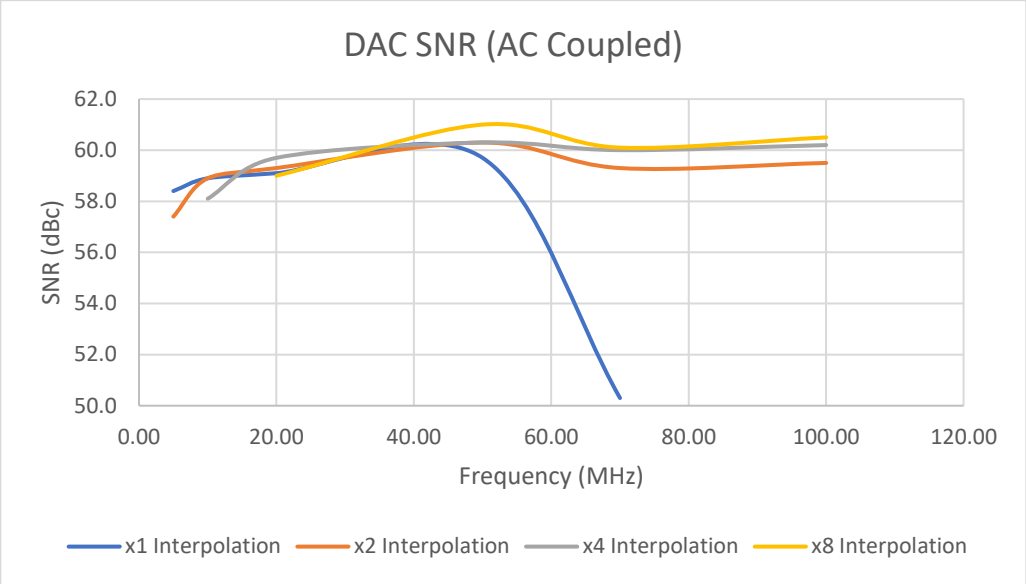
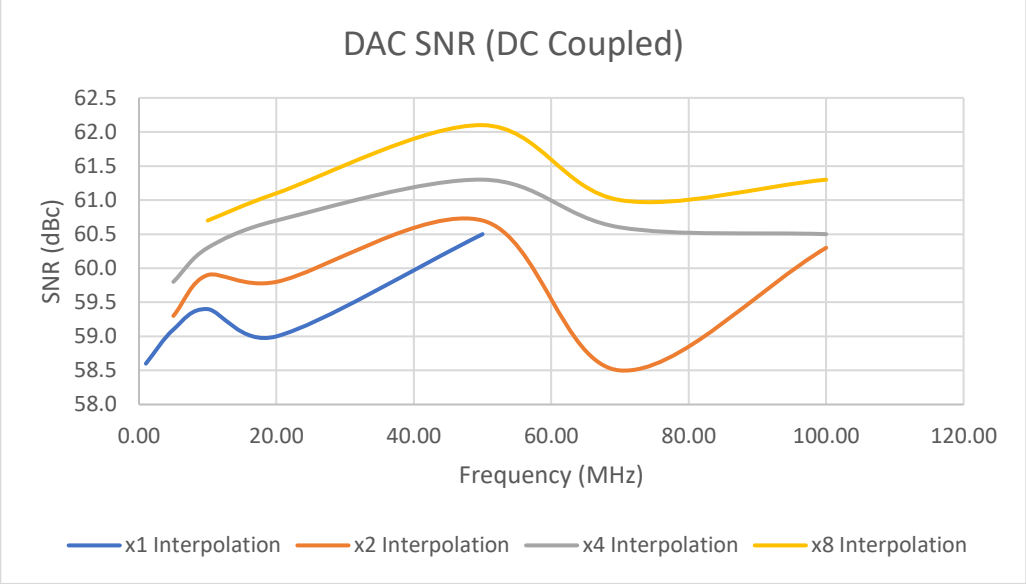
	ELECTRICAL CHARACTERISTICS Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.				
Group	**Parameter**	**Cfg.**	**Typ**	**Units**	**Notes**
Analog Outputs	-3dB Bandwidth	-0	5 - 110	MHz	AC coupled
		-1	0 - 110	MHz	DC coupled
	SFDR	-0	73	dBc	AC coupled, 5 MHz Output, FS = 250 MSPS, x1 Interpolation, 95% FS
		-1	62	dBc	DC coupled, 5 MHz input, FS = 250 MSPS, x1 Interpolation, 95% FS
	SNR	-0	58	dBc	AC coupled, 5 MHz Output, FS = 250 MSPS, x1 Interpolation, 95% FS
		-1	59	dBc	DC coupled, 5 MHz input, FS = 250 MSPS, x1 Interpolation, 95% FS
	THD	-0	-70	dB	AC coupled, 5 MHz Output, FS = 250 MSPS, x1 Interpolation, 95% FS
		-1	-60	dB	DC coupled, 5 MHz input, FS = 250 MSPS, x1 Interpolation, 95% FS
	ENOB	-0	9.1	Bits	AC coupled, 5 MHz Output, FS = 250 MSPS, x1 Interpolation, 95% FS
		-1	8.6	Bits	DC coupled, 5 MHz input, FS = 250 MSPS, x1 Interpolation, 95% FS
	Channel Crosstalk	All	< -80	dB	70 MHz output, FS = 250 MSPS, 98% FS. Adjacent Channel
	Noise Floor	All	< -88	dB	AC and DC Coupled
	Gain Error	All	< 1	% of FS	Calibrated
	Offset Error	All	< 1	mV	Calibrated
Power	Supply Current	All	3.5	A	Max
	Power Dissipation	All	17	W	Max
	Calibration Interval	All	1	year	

Typical DAC Performance





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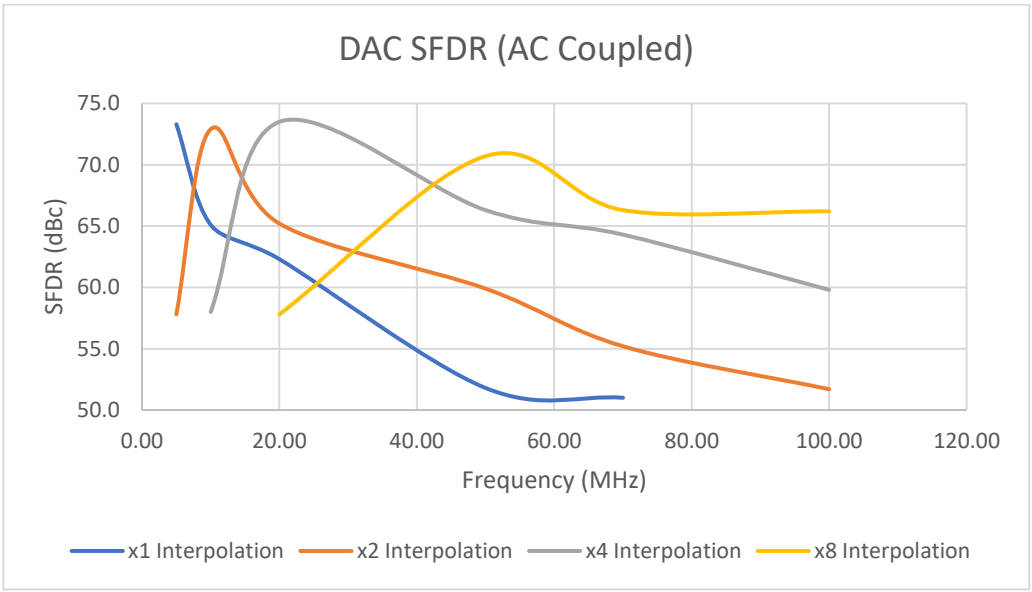

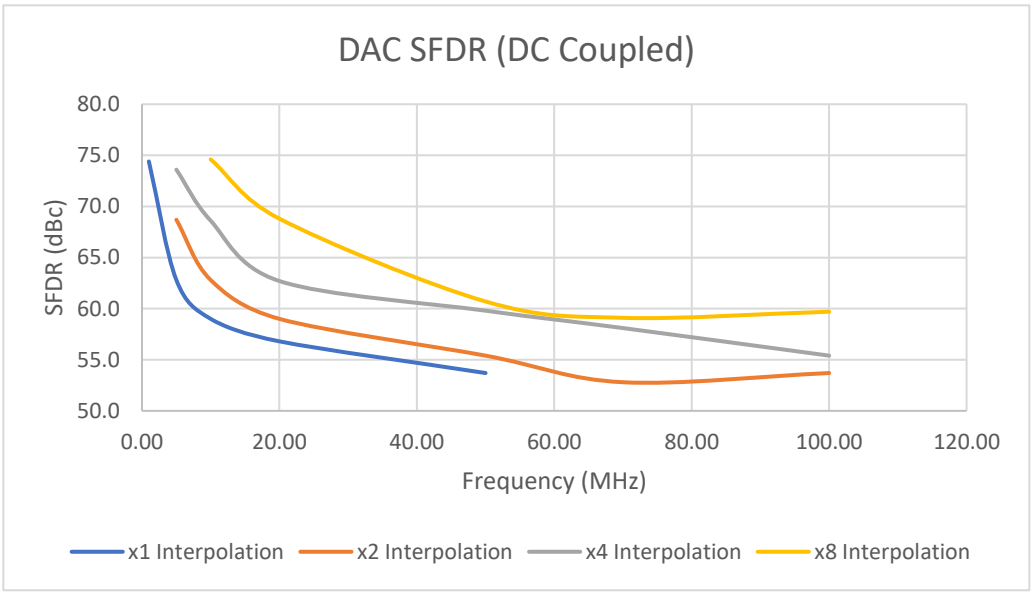

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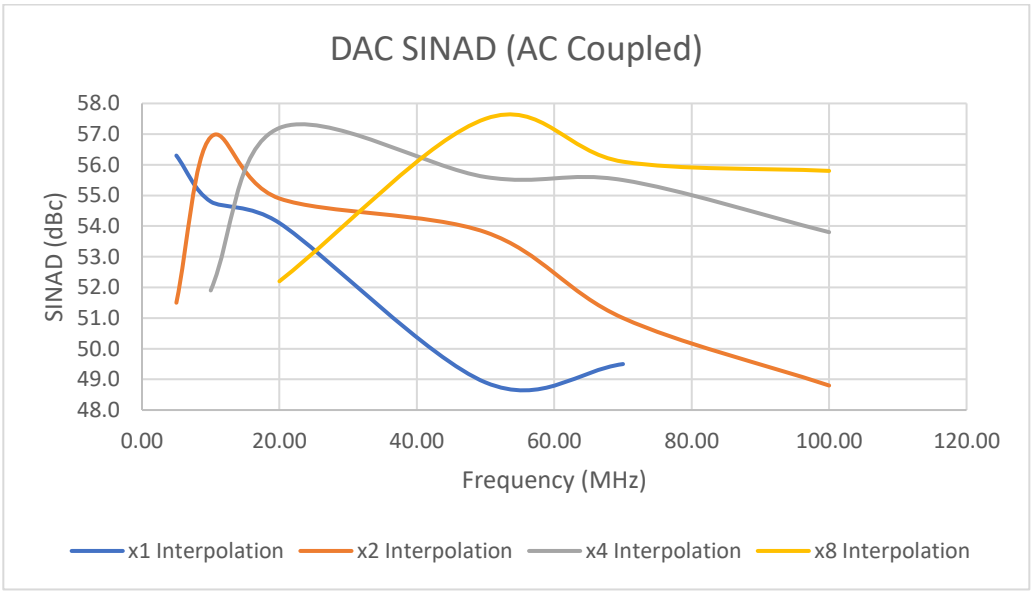

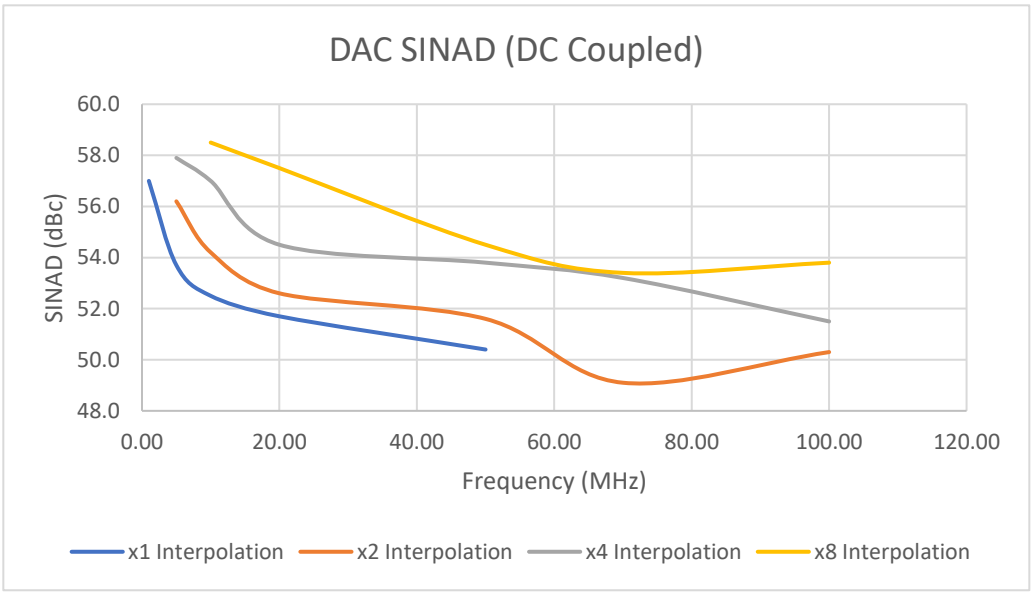

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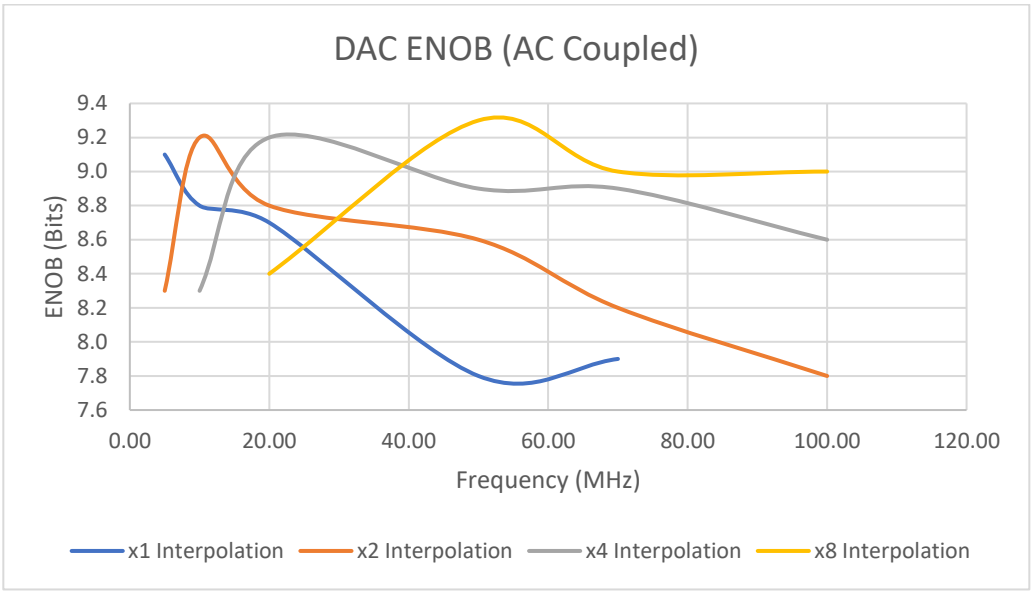
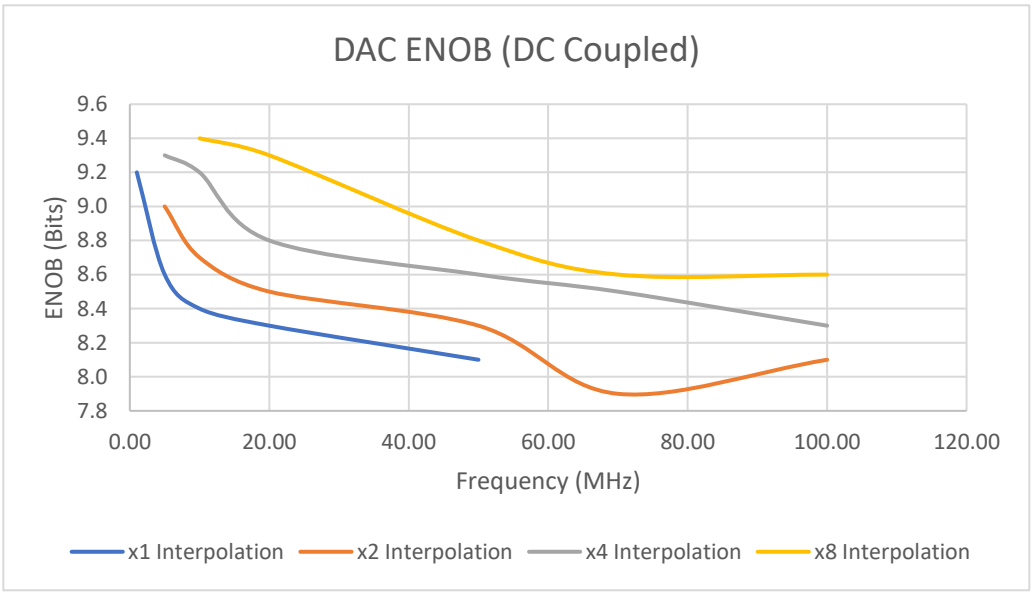

DAC ENOB (AC Coupled)
ENOB (Bits)
9.4
9.2
9.0
8.8
8.6
8.4
8.2
8.0
7.8
7.6
0.00
20.00
40.00
60.00
80.00
100.00
120.00
Frequency (MHz)
x1 Interpolation
x2 Interpolation
x4 Interpolation
x8 Interpolation


DAC ENOB (DC Coupled)
ENOB (Bits)
9.6
9.4
9.2
9.0
8.8
8.6
8.4
8.2
8.0
7.8
0.00
20.00
40.00
60.00
80.00
100.00
120.00
Frequency (MHz)
x1 Interpolation
x2 Interpolation
x4 Interpolation
x8 Interpolation

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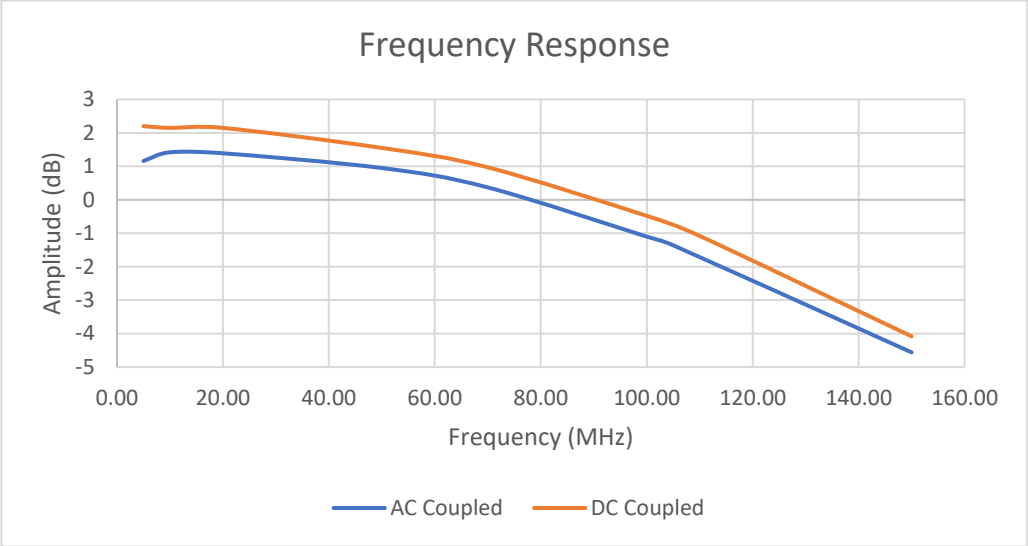

Architecture and Features

The XA-AWG module has eight analog outputs that are simultaneously sampling channels of 16-bit, 250 MSPS DAC output. The eight DAC channels have a ±0.5V or 1Vpp output range. Additional digital IO control bits from the FPGA are provided for application control and signaling.

Controls for triggering and clocks allow precise control over the collection of data. Trigger modes include frames of programmable size, external and software. Multiple XA-AWG cards can sample simultaneously using external trigger inputs with synchronized sample clocks. The sample clock can be external or generated from the on-card PLL. The PLL can either use the on-card 100 MHz reference, or can use an external reference. When an external reference is used, the sample clock is synchronous to the reference.

The XA architecture has a data buffering and packet system that provides efficient and flexible data transfers to the host computer. The data buffer uses the entire SDRAM memory in a single virtual FIFO mode. Data from both ADCs are interleaved into a single stream. Data is transferred to the host using the PCIe controller interface as data packets. The packet data system controls the flow of packets to the host, or other recipient, using a credit-based system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. The data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements for all types of applications.

The data acquisition process can be monitored using the XA alert mechanism. The alerts provide information on the timing of important events such as triggering, over ranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the XA modules easier to integrate into larger systems.

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Software Tools

Software for data logging and analysis are provided with every XA module. Data can be logged to system memory at full rate or to disk at rates supported by the drive and controller. Triggering, sample rate controls, and data logging features allow you to use XA modules in your application without ever writing code. Our software applications include *Binview* program which provides data viewing, analysis, and export data to MATLAB for large data files, as well as support applications for logic loading, firmware updates, and system configuration.

Software development tools for the XA modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high-speed data acquisition easier to integrate into applications. By default, Qt-Creator project files are provided to compile and build C/C++ applications on 64bit Windows or Linux operating systems. For additional support please contact our support.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the XA modules by modifying the logic. The FrameWork Logic tools support RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

Applications Information

Maximum Data Rates

The maximum data rates supported by the module are limited by the PCI Express transfer rate when the total data rate exceeds 1600 MB/s. The PCI Express transfer rate can reach up to 1600MB/s which does not allow full saturation of the ADC and DAC raw data rate.

It is important to qualify systems for performance when data rates exceeding 1600 MB/s are required.

Cables

The XA-AWG module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SSMC male connector and 50 ohm characteristic impedance for best signal quality.

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XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXIe using an adapter card. The adapter cards are software transparent.

The XA modules use the auxiliary P16 connector for digital IO and additional clock inputs. A total of 34 bits of digital IO, directly connected to the application FPGA, are routed to the J16 connector as 4 balanced differential pairs supporting LVDS or lower speed single-ended LVCMOS signals. The XA modules also have a sample clock input and PLL reference input to J16. The cPCI/PXIe adapter uses these to connect to system clocks, while the PCIe desktop adapter provides SMB input connectors for system clock inputs.

PCIe-XMC Adapter (80341) x8 PXIe to XMC Clock and trigger inputs	**PCIe-XMC Adapter (80260)** x8 VPX to XMC Conduction cooling	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC x8 RIO ports supported on P16
		
ASSY XMC-PCIe x8 ADAPTER (80363) x8 PCIe to XMC On-board USB to JTAG Programmer High speed expansion port (Mini-SAS, QSFP) Conduction Cooling External VPWR Power option available XMC Module Voltage and Current Test Header		
		

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Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with XA modules.

eInstrument PC with Dual PCI Express XMC Modules (90602) Windows/Linux embedded PC 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to XMCs 2000 MB/s, 4 TB datalogger 9-18V operation	**EPC-Nano (80342)** Windows/Linux Embedded Single Board Computer Extremely small form-factor Single XMC IO Site and 1 GbE Link 8-14Vdc operation
	

Usage and Market

The XA-AWG is a digital device and apparatus exclusively for use in business, industrial and commercial environments. The XA- AWG peripheral is not marketed, sold or otherwise made available for home or residential environment use.

The XA- AWG is exclusively for use with wired input and output signals. The XA- AWG peripheral is not an intentional radio transmitter or receiver and is not marketed, sold or otherwise made available for connection to wireless media (with an antenna, etc…).

The XA- AWG is not a “PC” (“personal” or “portable computer” marketed for home or residential environment use) or “PC” peripheral and is not marketed, sold or otherwise made available as a “PC” or “PC” peripheral.

The XA- AWG may be sold as a subassembly where the integrator/purchaser takes responsibility for their assembled digital device’s or apparatus’s compliance. Consult Molex for clarification and assistance.

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www.innovative-dsp.com

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