X6-GSPS

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Innovative Integration
... real time solutions!

XMC Module with Two 1.8 GSPS, 12-bit A/Ds, Xilinx Virtex-6 FPGA, and 4 GB LPDDR2

FEATURES

- Two 1.8 GSPS, 12-bit A/D channels/single channel interleaved at 3.6 GHz
- Input Bandwidth: 2.2 GHz
- 1 Vp-p, AC-coupled, 50 ohm, SMA inputs
- Xilinx Virtex-6 SX475T/SX315T/LX240T
- 4 banks of 1 GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCI Express providing 3.2 GB/s sustained transfer rates (-2 FPGA Required)
- Digital IO: 32-bits LVDS/64-bit LVCMOS
- Pulse repetition interval trigger mode
- XMC Module (75x150 mm)
- 26 W typical
- Conduction cooling per VITA 20
- Ruggedization Levels for wide temperature and Vibration/Shock
- Adapters for VPX, Compact PCI, desktop PCI and cabled PCI Express systems

APPLICATIONS

- Wireless Receiver
- WLAN, WCDMA, WiMAX front end
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux/VxWorks Drivers
- C++ Host Tools

XILINX®

MATLAB®

DESCRIPTION

The X6-GSPS integrates high-speed digitizing with signal processing on a PCI Express XMC IO module for demanding DSP applications. The tight coupling between the digitizing and the Virtex6 FPGA core is well suited for SDR, RADAR, and LIDAR front end sensor digitizing and processing. The PCI Express system interface sustains transfer rates over 2 GB/s for data recording and integration as part of a high performance realtime system.

The X6-GSPS features two, 12-bit 1.8 GSPS A/Ds that can be interleaved to use as one 3.6 GSPS digitizer. Analog input bandwidth of over 2 GHz supports wideband applications and undersampling. The sample clock is from either a low-jitter PLL or external input. Multiple cards can be synchronized for sampling and down-conversion.

A Xilinx Virtex6 SX315T (LX240T and SX475T options) with 4 banks of 1GB DRAM provide a very high performance DSP core with over 2000 MACs (SX315T). The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates.

The X6-GSPS power consumption is 25W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

The FPGA logic can be fully customized using VHDL and MATLAB using the Frame Work Logic tool set. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator. IP cores for many wireless, DSP and RADAR functions such as large-scale preintegrator, DDC, PSK/FSK demod, OFDM receiver, correlators and large FFT are available.

Software tools for host development include C++ libraries and drivers for Windows, Linux and VxWorks. Application examples demonstrating the module features are provided.

X6-GSPS

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X6-GSPS	80264- <CFG> -<ER>	XMC module with two 1.8 GSPS, 12-bit A/Ds, Virtex-6 FPGA, 4GB DRAM. <CFG> is Configuration. **0**: LX240T1, Gen1, AC-Coupled, **1**: LX240T2, Gen2, AC-Coupled, **2**: SX315T1, Gen1, AC-Coupled, **3**: SX475T1, Gen1, AC-Coupled, **4**: SX475T2, Gen2, AC-Coupled, **5**: SX315T2, Gen2, AC-coupled, <ER> is environmental rating **L0...L4**.
Logic Development Package		
X6-GSPS FrameWork Logic	55036	X6-GSPS FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC-PCI Adapter	80167-0	PCI carrier card for XMC PCI Express modules, 64-bit PCI
XMC-PCIe Adapter	80259-0	PCI Express carrier card for XMC PCI Express modules, x8 lanes
XMC-Compact PCI/PXI Adapter	80207	3U compact PCI carrier card for XMC PCI Express modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
XMC-Cabled PCIe Adapter	90181-1	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
VPX Adapter	80262	3U VPX adapter for X6. Air-cooled or conduction-cooled versions. REDI covers available.
Embedded PC Host		
eInstrument-PC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Intel i7 CPU; Windows, Linux
eInstrument-PC-Atom low-power embedded PC XMC host	90201	Embedded PC with support for two XMC modules; Intel Atom or i7 CPU; Windows, Linux
VPXI-ePC: 3U VPX PC with 4 expansion slots	90271	3U VPX embedded PC with 4 expansion slots, integrated timing and data plane; Intel i7 CPU; Windows, Linux

Heatsinks		
Standard Adapter (VPX, PXIe, DAQ-Node, eInstrument-PC, XMC-PCIe Adapter)	61548-1	Assembly, Heatsink Hardware, X6, XA on PXIe, VPX, ePC, DAQ-Node, XMC-PCIe Adapter
Standard Adapter (ePC-Duo)	Not Needed	EPC-Duo has the correct heatsinks installed.
Standard Adapter (SBC-Nano)	61543-1	Assembly, Heatsink Hardware, X6, XA on ePC-Nano

X6-GSPS

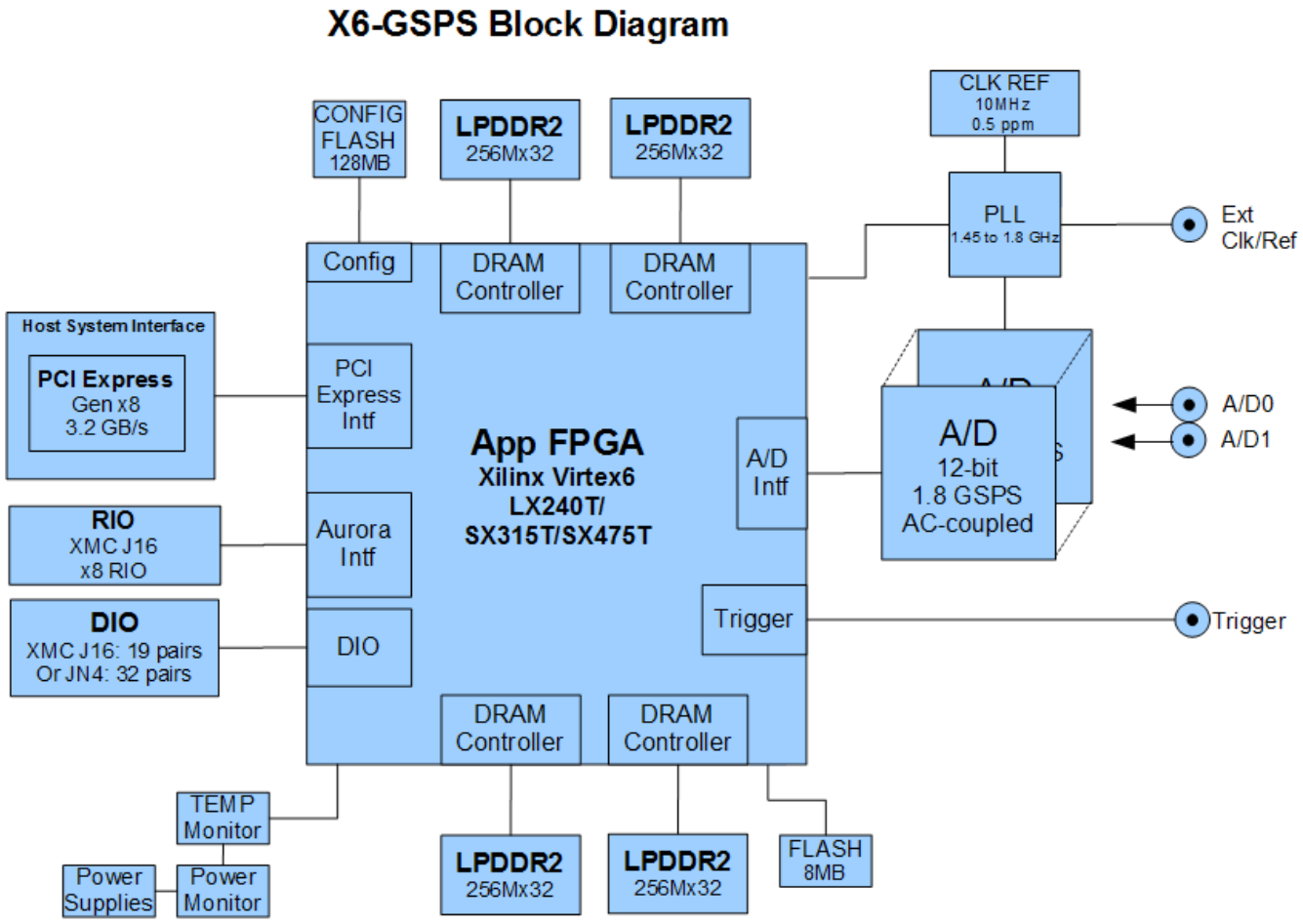


Figure 1. Block diagram

Operating Environment Ratings

X6 modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance. Click this link "Ruggedization Levels" to see the Ruggedization Levels available.

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

X6-GSPS

Standard Features

Analog	
Inputs	2
Input Range	1 Vp-p,
Max RF Input	2 Vp-p, 10dBm
Input Type	Single ended, AC coupled
Input Impedance	50 ohm
A/D Device	National Semiconductor ADC12D1800
A/D Resolution	12-bit
A/D Sample Rate	300 MHz to 1.8 GHz (Channels may be interleaved for one channel sampling at 3.6GHz)
Input Bandwidth	5 MHz to 2.2 GHz (-3dB)

FPGA	
Device	Xilinx Virtex-6
Speed Grade	-1 or -2
Size	SX315T : ~31M gate equivalent
Flip-Flops	SX315T: 393K
Multipliers	SX315T: 1,344
Slice	SX315T: 49,200
Block RAMs	SX315T: 1408 (25344 Kbits)
Rocket IO	16 lanes @ 5 Gbps (-1 speed)
Configuration	JTAG or FLASH In-system reprogrammable

Memories	
DRAM Size	4 GB; 4 banks of 1 GB each
DRAM Type	LPDDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	Up to 6.42 GB/s transfer rate per bank (400 MHz clock)

X6-GSPS

Host Interface	
PCI Express	x8 Lanes, VITA 42.3 PCI Express Gen 2 (x4 for -1 speed FPGA, x8 for -2 speed FPGA)
PCI Express Sustained Rate	3.2 GB/s (Gen2 x8) 1.2 GB/s (Gen2 x4 or Gen1 x8)
Clocks and Triggering	
Clock Sources	PLL or External
	PLL: 1400 to 1800 MHz, and integer divisions thereof External: 300 to 1800 MHz
PLL Reference	External or 10MHz on-board 10 MHz ref is +/-250 ppb, -40 to 85C
PLL Resolution	100 KHz Tuning Resolution
Phase Noise	-120 dBc @ 100 KHz
Triggering	External, software, acquire N frame, Repeated interval
Ext Trigger Timing	Rise time < 1.0 uS
Ext Trigger Level	0.5 – 2.5 Vp-p
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.
Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

Application IO (J4/J16)	
GTP Lanes	8 (J16) (lane is two wire pairs: TX/RX)
GTP data rate	5 Gbps/lane (4 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	32 (J16/J4)
Signal Standard	LVCMOS (2.5V) – NOT 3.3 compatible
Drive	+/-12 mA
Connectors	PMC J4/XMC J16

Power	
Power Consumption	26W (VPWR = 12V, 4 DDR banks, all Aurora ports, 8 lane PCIe)
Required Supplies	3.3V, 5-12V
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant

ELECTRICAL CHARACTERISTICS

At 24C ambient.

Parameter	Typ	Units	Notes
Analog Input Bandwidth	5 to 2200	MHz	-3dB
SFDR	58.6	dB	498 MHz sine input, 95%FS, Fs = 1.8 GSPS
S/N	53.1	dB	498 MHz sine input, 95%FS, Fs = 1.8 GSPS
THD	-56.6	dB	498 MHz sine input, 95%FS, Fs = 1.8 GSPS
ENOB	8.3	bits	498 MHz sine input, 95%FS, Fs = 1.8 GSPS
Channel Crosstalk	-85	dB	867 MHz, 1 Vp-p on adjacent channels
Noise Floor	-85	dB	Input Grounded, Fs = 1800 MSPS, 64K sample FFT, non-averaged
Gain Error	< 0.2	% of FS	Calibrated
Offset Error	< 5	mV	Calibrated
Power Consumption	26	W	VPWR = 12 V, 4 DDR banks, all Aurora ports, 8 lane PCIe; standard logic as delivered in Framework Logic package.

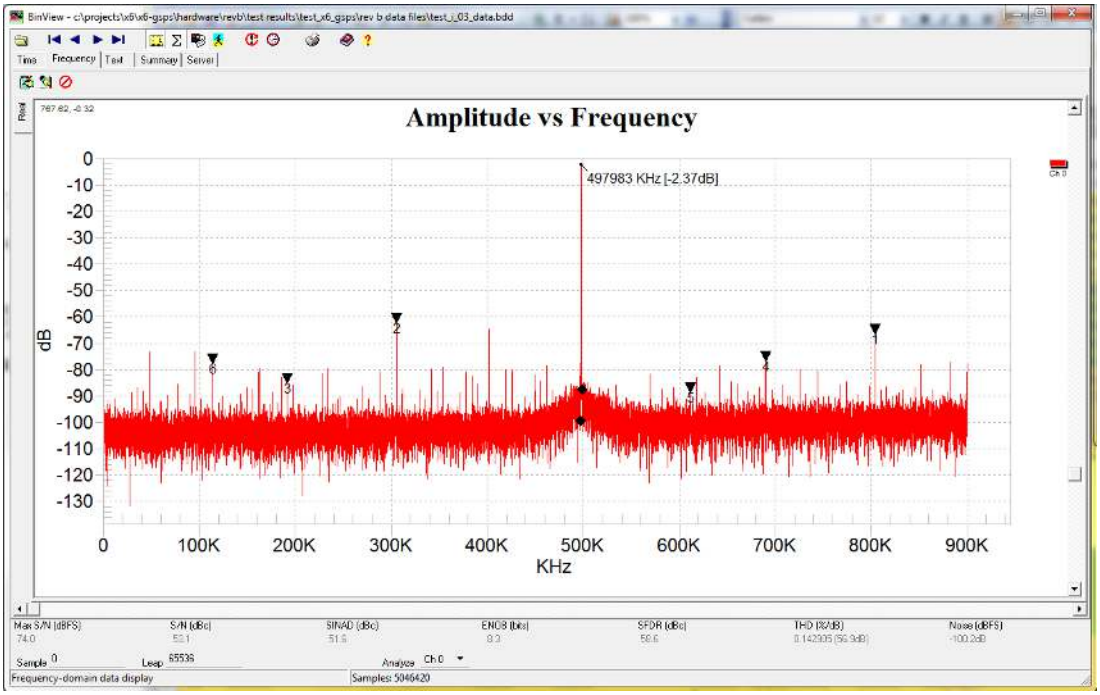


Figure 2. X6-GSPS A/D Performance, Fin = 498 MHz, Fs = 1800MHz, 342 mVRMS input

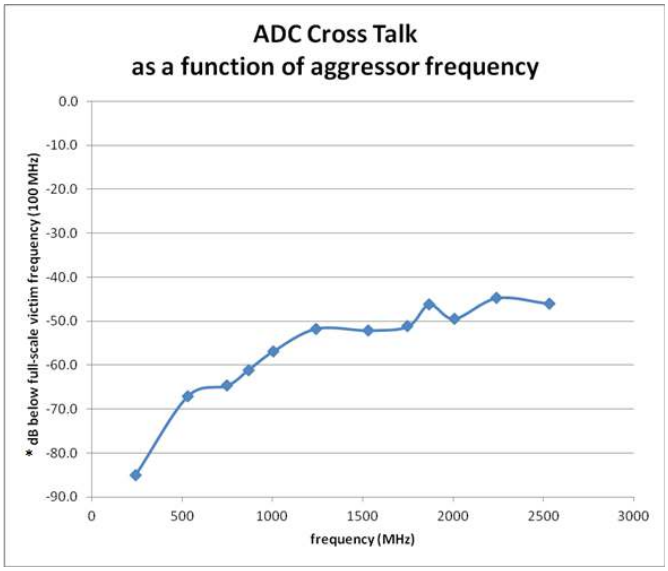


Figure 3. ADC Cross Talk as a function of aggressor frequency

*Note: ADC under observation (victim) had a constant full-scale 100 MHz tone. Neighboring ADC (aggressor) had full-scale tone at the frequencies shown along x-axis.

X6-GSPS

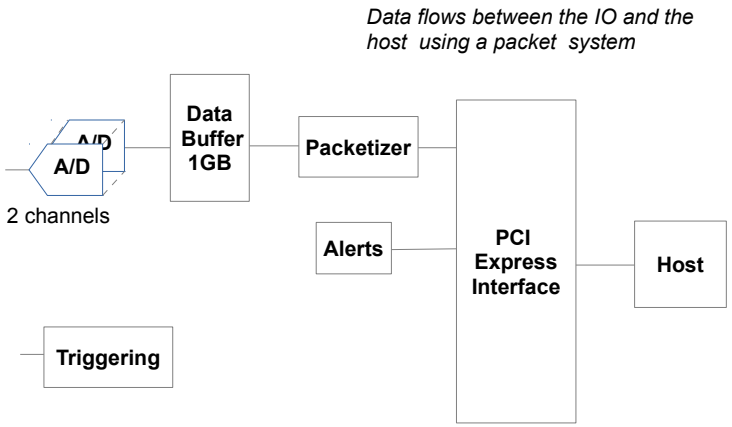
Architecture and Features

The X6-GSPS module architecture integrates analog IO with an FPGA computing core, memories and PCI host interface. This architecture tightly couples the FPGA to the analog for real-time signal processing with low latency and extremely high rates. As as result, the X6-GSPS is an ideal front-end for demanding applications in wireless, RADAR and medical imaging.

Analog IO

The analog front end of the X6-GSPS module has two simultaneously sampling channels of 12-bit, 1.8 GSPS A/D input. The A/D channels can be used in an interleaved mode as one channel of 3.6 GSPS. The A/D inputs have an analog input bandwidth of over 2 GHz for wideband and direct sampling applications.

The A/Ds are directly connected to the FPGA for minimum data latency. In the standard logic, the A/Ds have an interface component that receives the data, provides digital error correction, and a FIFO memory for buffering. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.



X6 Architecture

The A/D channels operate synchronously for simultaneously sampling systems using the external clock input. Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include triggering at a programmable interval for pulse repetition applications, frames of programmable size, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized in the logic to accommodate a variety of triggering requirements.

FPGA Core

The X6 Module family has a Virtex6 FPGA and memory at its core for DSP and control. The Virtex6 FPGA is capable of over 1 Tera MACs (SX315T operating at 500 MHz internally) with over 1300 DSP elements in the SX315T FPGA. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to four banks of 1GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like image analysis. Memory controller IP for circular buffering, pattern generation and multiple queues are available for application work.

The X6 module family uses the Virtex6 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. Logic utilization is typically <10% of the device.

PCI Express Host Interface

The X6 architecture delivers over 2 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is

transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. The data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex6 FPGA using 8 GTP (Gigabit Transceiver Ports), for a maximum bit rate of over 40 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 400 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

System Data Plane Ports and Digital IO

The X6 module family has eight high speed serial data links on J16 for system interconnect, operating at up to 5 Gbps per link, full duplex. These links enable the X6 modules to integrate into switched fabric systems such as VPX to create powerful computing and signal processing architectures. The standard logic uses these lanes as two Aurora ports of 4 lanes each. Other protocols such as SRIO and SPDP may be implemented in the FPGA.

J4 connector has 64 digital lines that connect to the FPGA. These signals are routed as differential pairs, supporting data rates with LVDS up to 1 GHz.

Module Management

The X6 family has independent temperature monitoring for the FPGA die. The temperature sensor is set so that power shuts when a critical temperature is exceeded. This function is independent of the FPGA.

The data acquisition process can be monitored using the module alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the card easier to integrate into larger systems.

FPGA Configuration

The modules uses a FLASH memory for the Virtex 6 FPGA image. This FLASH can be programmed in-system using a software applet. There are two images in the FLASH: an application image and a backup image.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable.

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Software Tools

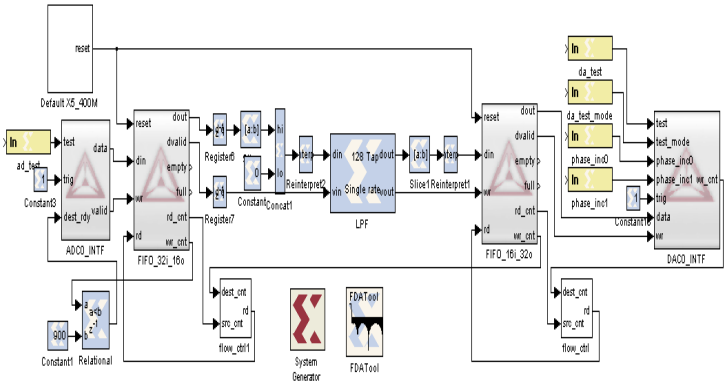
Software development tools for the module provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for the Microsoft, Embarcadero and GNU C++ toolchains is provided. Supported OSes include Windows, Linux and VxWorks. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the module by modifying the logic. The FrameWork Logic tools provide support for VHDL\Verilog and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designers build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



Using MATLAB Simulink for Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

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Digital Receiver

Digital Receiver is a turnkey solution providing integrated data logging, digital down-conversion (DDC), spectrum analyzer (FFT) in the compact system. The solution consists of three parts: the FPGA-based analog digitizer module, an eInstrument PC, and the firmware/software package to capture and analyze the data immediately.

A development kit is available to support creation of advanced custom firmware by logic developers. Netlist versions of the IP cores used to build the Digital Receiver are provided, so developers can integrate with their own custom cores to create an enhanced receiver design.

Product	DDC	FFT
V603	8 channels; bandwidth: 10 KHz – 50 MHz	1ch, 32K
V604	1 channel; bandwidth: 60 – 750 MHz	1ch, 32K

Table 1. Digital receivers

Part Number	Target Module	Product	Description
55201-1	X6-GSPS	UWB DDC and Spectrum Analysis	Framework Logic - 1 channels of IP-UWBDDC and 1 channel of IP-FFT32K for Virtex-6 SX475T2
55201-2	X6-GSPS	DDC and Spectrum Analysis	Framework Logic - 8 channels of IP-DDC-2GSPS and 1 channel of IP-FFT32K for Virtex-6 SX475T2

Table 2. Development kits

Part Number	Target Module	Product	Description
55101-1	X6-GSPS	UWB DDC and Spectrum Analysis	Package - 1 channels of IP-UWBDDC and 1 channel of IP-FFT32K for Virtex-6 SX475T2
55101-2	X6-GSPS	DDC and Spectrum Analysis	Package - 8 channels of IP-DDC-2GSPS and 1 channel of IP-FFT32K for Virtex-6 SX475T2

Table 3. Software/firmware package

X6-GSPS

Cables

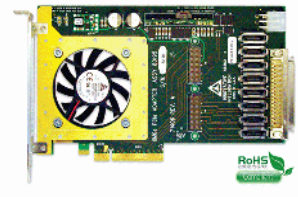
The X6-GSPS module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality.

XMC Adapter Cards

XMC modules can be used in standard desktop, VPX or or compact PCI/PXI systems using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The adapters provide support for using the GTP ports on P16 for private communications as well as access to the digital IO. The two adapters for desktop/server applications (80173 and 80259) can be used in "patch-panel" fashion to interconnect cards. The VPX adapter presents these ports to the VPX backplane on ports A-B or C-D.

The VPX adapter supports 3U air-cooled or conduction-cooled applications. The adapter has steering for ports A-C and IPMI support. REDI covers for 2-level maintenance applications are also available.

PCIe-XMC Adapter (80172) x1 PCIe to XMC Clock and trigger inputs 	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC P16 x8 RIO ports to SATA2 connectors DIO to MDR68 	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC P16 x8 RIO ports to SATA connectors Jn4 DIO to MDR68 Preferred for X6 	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC 
VPX-XMC Adapter (80262-6) 3U conduction-cooled VPX adapter Configurable port A-D mapping Optional REDI covers 	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 		

X6-GSPS

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X6 modules. The VPXI system supports multiple card systems with integrated timing and data plane features.

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)

Windows/Linux embedded PC
Intel Core2Duo or low power Atom available
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
100 MB/s, 400 GB datalogger
9-18VDC operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent
Supports standalone operation for X6 modules

3U VPX PC with Four Expansion Slots and Integrated Timing (90271)

3U VPX, air-cooled chassis with backplane
Runs Windows, Linux, VxWorks
Intel Dual Core i5 or i7, 8GB, 256MB SSD
4x USB, GbE, x8 cable PCIe, Displayport, T
Integrated timing clocks and triggers with GPS option
400 MB/s, 1TB datalogger
AC or DC operation

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