X6-400M

V2.2 01/06/22

INTERCONNECT SYSTEMS
a molex company

XMC Module with Two 400/500 MSPS A/Ds, Two 500 MSPS DACs, Xilinx Virtex-6 FPGA, 4 GB LPDDR2

FEATURES

- Two 400 MSPS, 14-bit A/D channels (500MSPS, 12-bit option)
- Two 500 MSPS, 16-bit D/A channels
- Xilinx Virtex-6 SX475T/SX315T/LX240T
- 4 banks of 1 GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCI Express providing 3.2 GB/s sustained transfer rates (-2 FPGA Required)
- Digital IO: 32-bits LVDS/64-bit LVCMOS
- XMC module (75x150 mm)
- 22 – 28 W typical
- Conduction cooling per VITA 20
- Ruggedization Levels for wide temperature and Vibration/Shock
- CE and FCC certified
- Adapters for VPX, Compact PCI, desktop PCI and cabled PCI Express systems

APPLICATIONS

- Wireless Receiver and Transmitter
- LTE, WiMAX Physical Layer
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ DevKit

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DESCRIPTION

The X6-400M integrates 400 MSPS data conversion with high performance signal processing on an XMC IO module for demanding DSP applications. The tight coupling of the data converters to the Virtex6 FPGA core realizes architectures for SDR, RADAR, and LIDAR front end sensor digitizing and processing. The PCI Express system interface sustains transfer rates over 2.8 GB/s for data recording and integration as part of a high performance real-time system.

The X6-400M features two 14-bit, 400 MSPS or two 12-bit 500 MSPS A/Ds, either AC or DC-coupled, plus two 500 MSPS update rate DACs. The DAC can be used as a single 1 GHz output channel. Analog IO is either AC or DC coupled. Receiver IF frequencies of up to 250 MHz are supported. The sample clock is sourced from a low-jitter PLL or an external clock/reference. Multiple boards offer coherent sampling as well as up and down-conversion.

A Xilinx Virtex-6 SX475T with 4 banks of 1GB DRAM provides a very high performance DSP core with over 2000 MACs. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates.

The X6-400M power consumption is 19W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate.

The FPGA logic can be fully customized using VHDL using the Frame Work Logic DevKit.

A software development kit for host development includes C++ libraries and 64-bit drivers for Windows and Linux. An application demonstrating the module's features, including streaming DAC samples from disk, is provided.

X6-400M

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X6-400M		PMC/XMC module with two 400 MSPS, 14-bit A/Ds, two 500 MSPS DACs, Virtex-6 FPGA, 4GB DRAM
	80270-2	X6-400M with LX240T-2 Speed FPGA, A/Ds AC-Coupled
	80270-3	X6-400M with LX240T 2 Speed, 500 MSPS A/D's, AC-Coupled A/D and D/A
	80270-6	X6-400M with LX240T FPGA 2 Speed, DC-Coupled A/D and D/A
	80270-8	X6-400M with SX475T2 FPGA Speed 2, DC-Coupled
	80270-10-L0	X6-400M with SX475T2 FPGA Speed 2, AC-Coupled
	80270-11	X6-400M with SX315T2 Speed 2 FPGA AC-Coupled A/D and D/A
	80270-12	X6-400M with SX315T2 FPGA, PCIe 8-lane gen 2, DC-Coupled
	80270-14	X6-400M with SX315T2 FPGA, 8 Lane FPGA GEN2, AC-Coupled, 12 Bit 500 MSPS A/D
		Environmental Rating -L1, -L2, -L3 or -L4 available upon request.
Logic Development Package		
X6-400M FrameWork Logic	55034	X6-400M FrameWork Logic board support package for RTL. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC-PCIe x8 Adapter		PCI Express carrier board for XMC modules, x8 lanes, Onboard USB JTAG, Robust Thermal Solution, Voltage Monitor, 8 high quality Differential DIO pairs, High speed expansion port (QSFP)
	80363-0-L0	XMC-PCIe X8 ADAPTER X6 HIGH HEAT INT PWR
	80363-1-L0	XMC-PCIe X8 ADAPTER X6 HIGH HEAT EXT PWR
	80363-2-L0	XMC-PCIe X8 ADAPTER XMC INT PWR
	80363-3-L0	XMC-PCIe X8 ADAPTER XMC EXT PWR
XMC-PXIe Adapter		PXIe carrier carrier board for XMC modules, x8 lanes, 8 High Speed gigabit transceiver (QSFP), 8 high quality Differential DIO pairs
	80341-1-L0	XMC-PXIE Adapter Full Feature X6 3U 8HP
	80341-5-L0	XMC-PXIe Adapter Full Feature X6 3U 8HP 32 DIO
XMC-PCIe Adapter		PCI Express carrier board for XMC modules, x8 lanes, JN4 connector with 32 standard Differential DIO pairs
	80259-1	PCIe-XMCe Adapter(eight lane) for X6 XMC modules

XMC-compact PCI/PXI Adapter	80207	3U compact PCI carrier board for XMC modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
DAQ Node	90181-1	Cabled PCI Express carrier board, x1 lane, XMC enclosure eINSTRUMENT DAQ NODE, X6
3U VPX Adapter	80260-0	VPX carrier board for XMC modules, x4 lanes, Conduction-cooled, DIO configurable for JN4 or P16 connector
Embedded Computer Hosts		
ePC-Duo	90602 See datasheet for options	ePC-Duo: Carrier Board for x2 XMC module, x8 lane, Skylake Processor, 32GB RAM, x1 1 Gbe, x2 10 Gbe, x4 mSATA, IEEE or GPS optional, x2 QSFP ports, Onboard USB JTAG (XMC module must have JTAG signals on P16 XMC connector), onboard voltage monitor, x10 high quality XMC module DIO pairs from each XMC module, convection-cooled chassis, 150W power supply
SBC-Nano	90654-0-L0	SBC-Nano: Carrier Board for x1 XMC module, COM Express Type 10 ATOM, 8 GB DDR3L memory, x4 lanes PCIe, x2 mSATA, x1 Gbe, Conduction or Convection cooled chassis

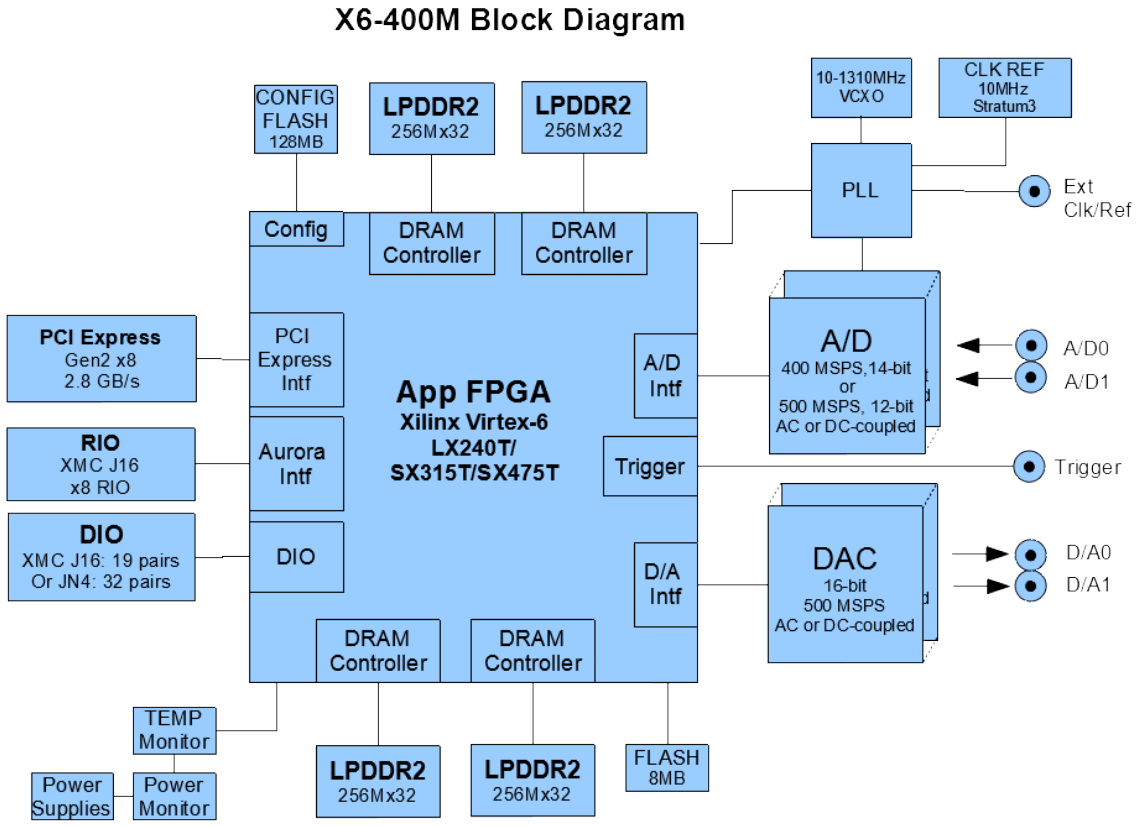
Figure 1. Block diagram

Operating Environment Ratings

X6 modules may be qualified for wide temperature, vibration and shock environmental ratings to suit a variety of applications.

Minimum lot sizes and NRE charges may apply. Contact ISI sales (ISISales@molex.com) for pricing and availability.

X6-400M


X6-400M Block Diagram
CONFIG FLASH 128MB
LPDDR2 256Mx32
LPDDR2 256Mx32
10-1310MHz VCXO
CLK REF 10MHz Stratum3
PLL
Ext Clk/Ref
Config
DRAM Controller
DRAM Controller
PCI Express Gen2 x8 2.8 GB/s
PCI Express Intf
App FPGA
Xilinx Virtex-6 LX240T/ SX315T/SX475T
A/D Intf
A/D
400 MSPS,14-bit or 500 MSPS, 12-bit AC or DC-coupled
A/D0
A/D1
RIO
XMC J16 x8 RIO
Aurora Intf
Trigger
Trigger
DIO
XMC J16: 19 pairs Or JN4: 32 pairs
DIO
D/A Intf
DAC
16-bit 500 MSPS AC or DC-coupled
D/A0
D/A1
DRAM Controller
DRAM Controller
TEMP Monitor
Power Supplies
Power Monitor
LPDDR2 256Mx32
LPDDR2 256Mx32
FLASH 8MB

X6-400M

Standard Features

Analog Input	
Inputs	2
Input Range	2 Vp-p (DC-coupled) 2.2 Vp-p (AC-coupled)
Input Type	Single ended, AC or DC coupled
Input Impedance	50 ohm
A/D Device	Texas Instruments ADS5474 (400MSPS, 14-bit) Texas Instruments ADS5463 (500MSPS, 12-bit)
A/D Resolution	14-bit or 12-bit
A/D Sample Rate	20 MHz to 400 MHz (400MSPS version) 20 MHz to 500 MHz (500MSPS version)
Input Bandwidth	5 MHz to 1000 MHz (-3dB) (AC-Coupled) DC to 250 MHz (-3dB) (DC-Coupled)

Analog Output	
Outputs	2
Output Range	0.9 Vp-p (AC-Coupled) 1 Vp-p (DC-Coupled)
Output Type	Single ended, AC or DC coupled
Output Impedance	50 ohm
DAC Device	Texas Instruments DAC5682Z
DAC Resolution	16-bit
DAC Update Rate	1000 MHz max, single channel mode; 500 MHz max, dual channel mode
Interpolation	None, 2x, 4x
Output Bandwidth	5 MHz to 350 MHz (-3dB) (AC-Coupled) 220 MHz (-3dB) (DC-Coupled)

FPGA	
Device	Xilinx Virtex-6
Speed Grade	-2 Speed Grade
Logic Cells	LX240T: 241,152 SX315T : 314,880 SX475T: 476,160
Multipliers	LX240T: 768 SX315T: 1344 SX475T: 2016
Slice	LX240T: 37680 SX315T: 49200 SX475T: 74400
Block RAMs	LX240T: 832 (14976 Kbiits) SX315T: 1408 (25344 Kbits) SX475T: 2128 (38304 Kbits)
Rocket IO	16 lanes @ 5 Gbps
Configuration	JTAG or FLASH In-system reprogrammable

Memories	
DRAM Size	4 GB; 4 banks of 1 GB each
DRAM Type	LPDDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	Up to 5.2 GB/s sustained transfer rate per bank (333 MHz clock)

X6-400M

Host Interface	
PCI Express	x8 Lanes, VITA 42.3 PCI Express Gen2 x8 Lane; (GEN1 x8 Lane for FPGA -1 Speed Grade)
PCI Express Sustained Rate	3.2 GB/s (x8 GEN2) 1.2 GB/s (x8 GEN1)

Clocks and Triggering	
Clock Sources	PLL or External
	0.3125 to 1000 MHz on-board PLL, external input is 0.1 Vp-p to 3.3 Vp-p, AC-Coupled, 50 ohm
PLL Reference	External or 10 MHz on-board 10 MHz ref is +/-250 ppb -40 to 85 C
PLL Resolution	100 kHz Tuning Resolution
Phase Noise	-130 dBc @ 100 kHz
Triggering	External, software, acquire N frame, Repeated Interval
Ext Trigger Timing	Risetime < 1.0 uS
Ext Trigger Level	0.5 – 2.5 Vp-p
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.
Latency	A/D: 36.5 fs cycles DAC: 94 fs cycles
Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

Application IO (J4/J16)	
Rocket IO Channels	8 (J16)
Rocket IO data rate	5 Gbps/lane (4 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	32 (J16/JN4)
Signal Standard	LVCMOS (2.5V) – NOT 3.3 compatible
Drive	+/-12 mA
Connectors	PMC JN4/XMC J16
Power	
Consumption	22W (VPWR = 5V, 2 DDR banks and no Aurora ports instantiated, 4 lane PCIe) 28W (VPWR = 12V, 4 DDR banks, all Aurora ports, 4 lane PCIe)
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)
Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant
Certifications	
CE (European Standards)	EN55022: 2006 + A1 : 2007 EN 61000-3-3: 1995 +A1: 2001 & A2 : 2005 EN 61000-3-2: 2006 EN 55024: 1998 + A1: 2001 & A2: 20003
FCC (USA)	Class B

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
A/D Channels			
Analog Input Bandwidth	250	MHz	-3dB, DC coupled inputs
	1000	MHz	-3dB, AC coupled inputs
Analog Input Passband Flatness	0.5	dB	0 to 100 MHz, DC coupled
	0.3	dB	0 to 200 MHz, AC coupled
Broadband SFDR	69	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	79	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
SFDR, 70 MHz Carrier +/-5 MHz Band	90	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	95	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
Harmonic Distortion	58	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	82.1	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
ENOB	10.1	bits	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	10.9	bits	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
S/N	62.7	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	67.3	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
Crosstalk	- 91/ - 100	dB	Measured channel grounded with a 101 MHz, 95% FS sine input on other channel (DC/AC coupled)
Noise Floor	-100	dB	Fin = 70 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
	-105	dB	Fin = 70 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
Offset Error	< 500	µV	Factory calibration, average of 64K samples after warm-up.
Gain Error	< 0.2	%	Factory calibration after warm-up.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

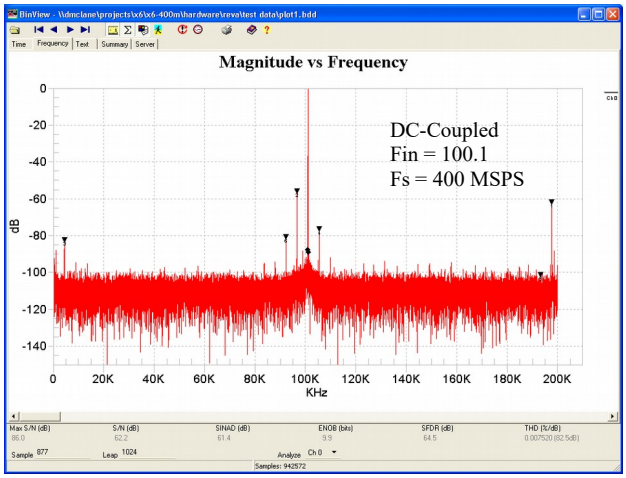
Parameter	Typ	Units	Notes
DAC Channels			
Analog Output Range	+/- 450	mV	Typical, AC coupled
	+/- 500	mV	Typical, DC coupled
Analog Output Bandwidth	220	MHz	DC coupled, no sin(x)/x compensation
	350	MHz	AC coupled, no sin(x)/x compensation
Output Amplitude Variation	0.7	dB	0 – 100 MHz, DC coupled, no sin(x)/x compensation
	0.8	dB	1 – 100 MHz, AC coupled, no sin(x)/x compensation
SFDR	66	dB	70.1 MHz sine output, 0 dBFS, AC coupled
	50	dB	70.1 MHz sine output, 0 dBFS, DC coupled
S/N	59.7	dB	70.1 MHz sine output, 0 dBFS, AC coupled
	58	dB	70.1 MHz sine output, 0 dBFS, DC coupled
THD	-62	dB	70.1 MHz sine output, 0 dBFS, AC coupled
	-49	dB	70.1 MHz sine output, 0 dBFS, DC coupled
Inter-modulation Distortion	< -75	dB	70 +/- 0.5 MHz, -6 dBFS, AC coupled
Noise floor	-100	dB	AC or DC output
Gain Error	< 0.02	% of FS	Calibrated
Offset Error	< 10	mV	Calibrated

RELIABILITY

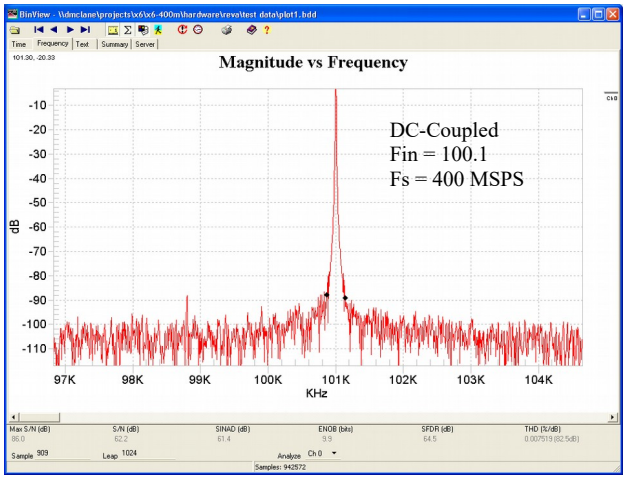
Failures/Million Hours	10.31
MTBF	96949.6 Hours

Note: Reliability data is based on normal enviromental conditions operating at and temperature of 50C.

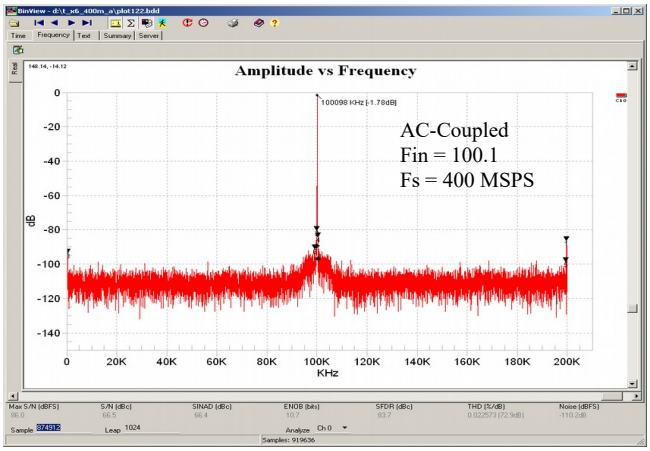
X6-400M



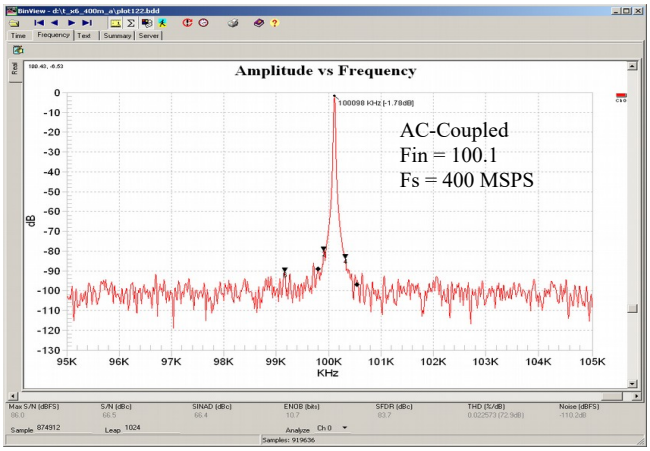
DC-Coupled A/D wideband signal quality, Fin = 101 MHz, Fs = 400 MHz on-board PLL. Channel 0, 15 pF parallel cap at A/D device inputs



DC-Coupled A/D narrowband signal quality, Fin = 101 MHz, Fs = 400 MHz on-board PLL. Channel 0, 15 pF parallel cap at A/D device inputs



AC-Coupled A/D wideband signal quality, Fin = 100.1 MHz, Fs = 400 MHz on-board PLL. Channel 0, 2.2 pF parallel cap at A/D device inputs



AC-Coupled A/D narrowband signal quality, Fin = 101 MHz, Fs = 400 MHz on-board PLL. Channel 0, 15 pF parallel cap at A/D device inputs

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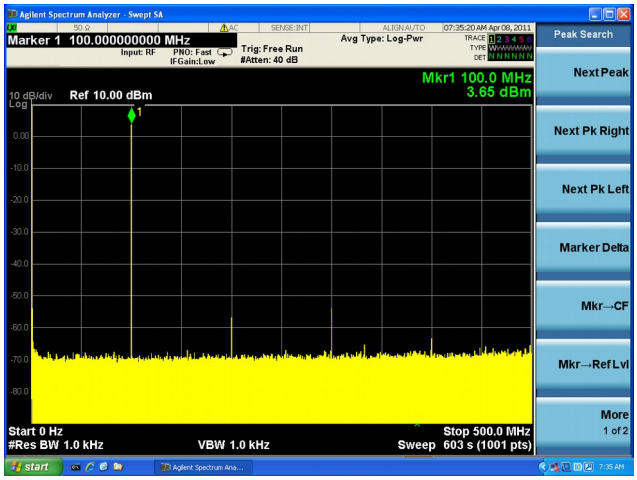
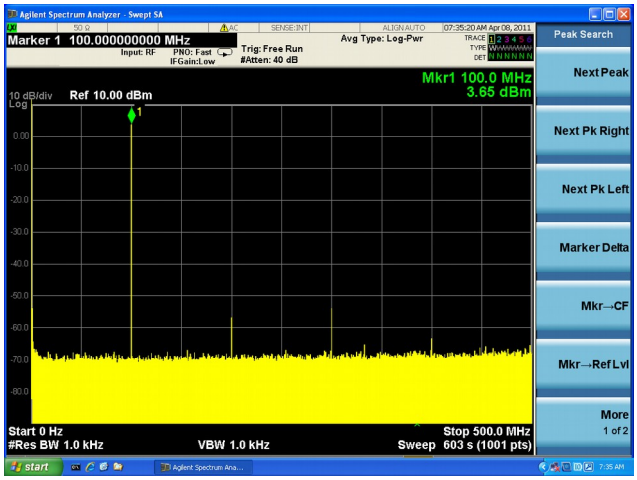


DC-Coupled output signal quality for Fout = 100.1 MHz, Fs = 1 GSPS.



AC-Coupled output signal quality for Fout = 100.1 MHz, Fs = 1 GSPS.

Architecture and Features

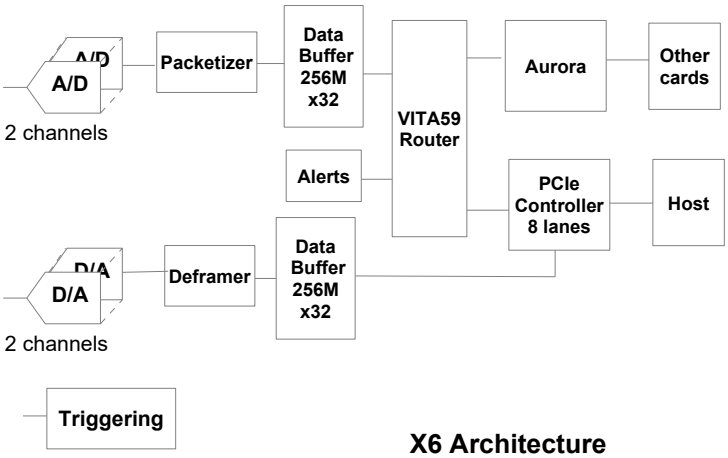
The X6-400M module architecture integrates analog IO with an FPGA computing core, memories and PCI host interface. This architecture tightly couples the FPGA to the analog signals for real-time signal processing with low latency and extremely high rates. The X6-400M is an ideal front-end for demanding applications in wireless, RADAR and medical imaging applications.

Analog IO

The analog front end of the X6-400M module has two simultaneously sampling channels of 14-bit, 400MSPS or 12-bit 500 MSPS A/D input and two channels of 500 MSPS 16-bit DAC output. The A/D inputs have an analog input bandwidth of up to 400 MHz for wideband and direct sampling applications.

The A/Ds are directly connected to the FPGA for minimum data latency. In the stock X6-400M Framework Logic, the A/Ds have an interface component that receives the data, performs digital calibration correction, and provides a FIFO memory for data buffering. A non-volatile ROM on the module stores factory-programmed, unique calibration coefficients for each data converter.

Data flows between the IO and the host or system using a packet system



X6 Architecture

The DAC is sourced directly from the FPGA with support for host data streaming over the PCIe bus or for arbitrary waveform generation (AWG) from the FPGA. In the AWG mode, a memory controller plays a dynamically linked list of data buffers residing in memory to the DAC at rates up to 500 MSPS or 1 GSPS (dual DAC configuration). The data buffers, along with their playback parameters are supplied by the host via PCIe or by the FPGA firmware. The playback parameters include gain level, number of repetitions to play, next buffer to play, and playback termination methods. The DAC also has optional interpolation modes of 2x, 4x or no interpolation. Coarse mixing functions permit the DAC to move the output to

several Nyquist zones.

A flexible set of trigger configuration modes, fully integrated with the FPGA logic, allows precise control over data acquisition and playback. Trigger start is initiated by an external trigger signal or via software command. Triggering may be specified as either edge or level sensitive, dependent on the source, and may be optionally programmed with user-defined frame sizes and repeat intervals. Multiple modules sample synchronously when the external trigger inputs are used with a common trigger signal. The trigger component in the FPGA VHDL is user-customizable to accommodate a variety of triggering requirements.

A non-volatile ROM is used to store the calibration coefficients for the front end analog and is programmed during factory test.

FPGA Core

The X6 Module family has a Virtex6 FPGA and memory at its core for DSP and control. The Virtex6 SX475 FPGA contains over 2000 DSP elements. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to four banks of 1GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The X6 module family uses the Virtex6 FPGA to integrate the module's components for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. FPGA resource utilization is typically <10% of the device.

PCI Express Host Interface

The X6 architecture delivers over 2.8 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides efficient and flexible DMA transfers at high data rates with minimal host support. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic which allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

System Data Plane Ports and Digital IO

The X6 module family has eight high speed serial data links on XMC connector J16 for system interconnect, operating at up to 5 Gbps per link, full duplex. These links enable the X6 modules to integrate into switched fabric systems such as VPX to create powerful computing and signal processing architectures. The standard Framework Logic implements these lanes as two Aurora ports of 4 lanes each. Other protocols such as SRIO and SFPDP may be implemented in the FPGA.

32 general purpose digital IO lines are available via 80259-0 Adapter JN4 connector. These lines connect directly to the FPGA. 16 general purpose digital IO lines (or 8 differential pairs) using a twinax cable are available on the 80363 Adapter Front Panel.

Module Management

The X6 family has independent temperature monitoring for the FPGA die. The temperature sensor is set so that power shuts

when a critical temperature is exceeded. This function is independent of the FPGA.

The data acquisition process can be monitored using the module alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert include an absolute system timestamp of the alert, and other information such as current temperature. This provides an overview of the module's data acquisition process by recording the occurrence of these real-time events making the module easier to integrate into larger systems.

FPGA Configuration

The module uses a FLASH memory for the Virtex 6 FPGA image. This FLASH can be programmed in-system using a software applet. There are two images in the FLASH: an application image and a "golden" image as a backup.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable.

Software Tools

Software development tools for the module provide comprehensive support including device drivers, data buffering, module controls, and utilities that allow developers to be productive. At the most fundamental level, the software library components deliver data buffers to the top-level application without the burden of low-level, real-time control of the module and its interface. Software classes provide C++ developers a powerful, high-level interface to the module that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's feature with a supplied application without ever writing code. Software applets include Binview which provides data viewing, analysis and import to MATLAB for large data files.

Support for the QtCreator and GNU C++ toolchains are provided. Microsoft Visual Studio toolchain is available by request. Supported OS's include Windows and Linux. For more information, the software tools User Guide and on-line help is available by request, contact Tech Support (ISItechsupport@molex.com).

Logic Tools

Custom DSP applications may be readily included in the module's FPGA. The standard Framework Logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the supplied components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project,.

X6-400M

The FrameWork Logic User Guide more fully detail the development tools. Some of the more important logic functions are shown here.

Logic Core	Description	Features
PCIe Interface	Interface to PCI Express bus supporting x1 to x8 lanes, Gen2. Implements Velocia packet system and Wishbone SOC bus.	Supports sustained data rates of up to 2 GB/s. Automates DMA transfers to the system using Velocia packet protocol. Wishbone SOC bus provides flexible bus architecture for designers.
Aurora Interface	Interface to x4 Aurora port for system expansion and data communicaitons.	Provides up to 1 GB/s data port to other cards for system expansion and data plane integration. Sub-channel support for messaging.
Router	Velocia packet router.	Dynamically steers packets amongst source and destination logic components.
Packetizer	Creates Velocia or VITA 49 packets.	Data packetizing and buffering for logic components for integration into Velocia packet system.
Deframer	Parses Velocia packets and dissembles them.	Deframer is used to extract data payloads from packets for logic component integration into Velocia packet system.

X6-400M

Digital Transceiver

Digital Transceiver for providing integrated data logging, playback, digital down-conversion (DDC), digital up-conversion (DUC), spectrum analyzer (FFT) are optionally available. The solution consists of three parts: the FPGA-based analog digitizer module, an Embedded PC, and the firmware/software package to capture and analyze the data immediately.

Contact ISISales@molex.com for more information.

X6-400M

Applications Information

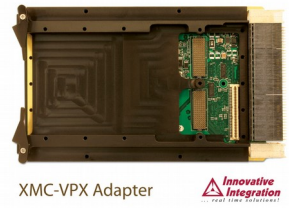
Cables

The X6-400M module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter board. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter boards allow the XMC modules to be used in any PCIe or PCI system.

The X6 module family uses the auxiliary XMC P16 connector as a private host interface. Eight high speed serial lanes with digital IO signals provide support for data transfer rates up to 4 GB/s sustained, as well as sideband signals for control and status. Protocols such as Aurora may be implemented for host communications or custom protocols.

ASSY XMC-PCIe x8 ADAPTER (80363) x8 PCIe to XMC On-board USB to JTAG Programmer High speed expansion port (Mini-SAS, QSFP) Conduction Cooling External VPWR Power option available XMC Module Voltage and Current Test Header 	PCIe-XMC Adapter (80341) x8 PXIe to XMC Clock and trigger inputs 	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC P16 x8 RIO ports to SATA connectors DIO to MDR68 	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC 
VPX-XMC Adapter (80262-6) 3U conduction-cooled VPX adapter Configurable port A-D mapping Optional REDI covers 	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 		

X6-400M

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X6 modules. The VPXI system supports multiple card systems with integrated timing and data plane features.

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)

Windows/Linux embedded PC
Intel Core2Duo or low power Atom available
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
100 MB/s, 400 GB datalogger
9-18VDC operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent
Supports standalone operation for X6 modules

3U VPX PC with Four Expansion Slots and Integrated Timing (90271)

3U VPX, air-cooled chassis with backplane
Runs Windows, Linux, VxWorks
Intel Dual Core i5 or i7, 8GB, 256MB SSD
4x USB, GbE, x8 cable PCIe, Displayport, T
Integrated timing clocks and triggers with GPS option
400 MB/s, 1TB datalogger
AC or DC operation

X6-400M

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