FMC-1000

V 0.992 06/08/16

FMC Module with 2x 1000 or 1250 Msps 14-bit A/D, 2x 1230 Msps 16-bit D/A Converters with PLL and Timing Controls

FEATURES

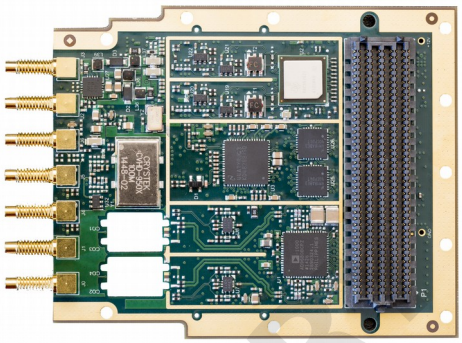
- Two A/D Inputs
  - Up to 1250* MSPS,14-bits each
  - AC or DC coupled
- Two D/A Outputs
  - Up to 1230* Msps,16-bits each 1x, to 2500* Msps with 4x interpolation
  - AC or DC coupled
- Sample clocks and timing and controls
  - Both front panel and FMC ports; DCLK, SYSCLK inputs, Trig/Sync/Monitor input/output, HW customizable
  - Programmable PLL
  - 25 MHz TCXO Reference
  - Integrated with FMC triggers
- FMC module, VITA 57.1
  - High Pin Count,
  - JESD204B (subclass 1) Interfaces
  - 2.5V Vadj
  - Power monitor and controls
- 10.4W typical (AC-coupled inputs)
- Conduction cooling supported
- Environmental ratings for -40 to 85C
  9g RMS sine, 0.1g2/Hz random vibration

APPLICATIONS

- Wireless Receiver and Transmitter
- LTE, WiMAX Physical Layer
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback

SOFTWARE

- MATLAB/VHDL FrameWork Logic



DESCRIPTION

The FMC-1000 is a high speed digitizing and signal generation FMC I/O module featuring two 1000* or 1250* MSPS A/D channels and two 1230* MSPS D/A channels supported by sample clock and triggering features.

Analog I/O may be either AC or DC coupled. The sample clock is from either an ultra-low-jitter PLL or can be derived from external inputs. Multiple cards can be synchronized for sampling.

The FMC-1000 power consumption is less than 10.4W for typical operation (AC coupled, 12W DC coupled). The module may be conduction cooled using provided thermal interfaces and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

Support logic in VHDL is provided for integration with FPGA carrier cards. Specific support for Innovative carrier cards includes integration with Framework Logic tools that support VHDL/Verilog and Matlab developers. The Matlab BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator for the FMC integrated with the FPGA carrier card.

Software tools for Innovative carrier cards include include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features are provided.

* Sampling rates in an application depend on carrier and system design

FMC-1000

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

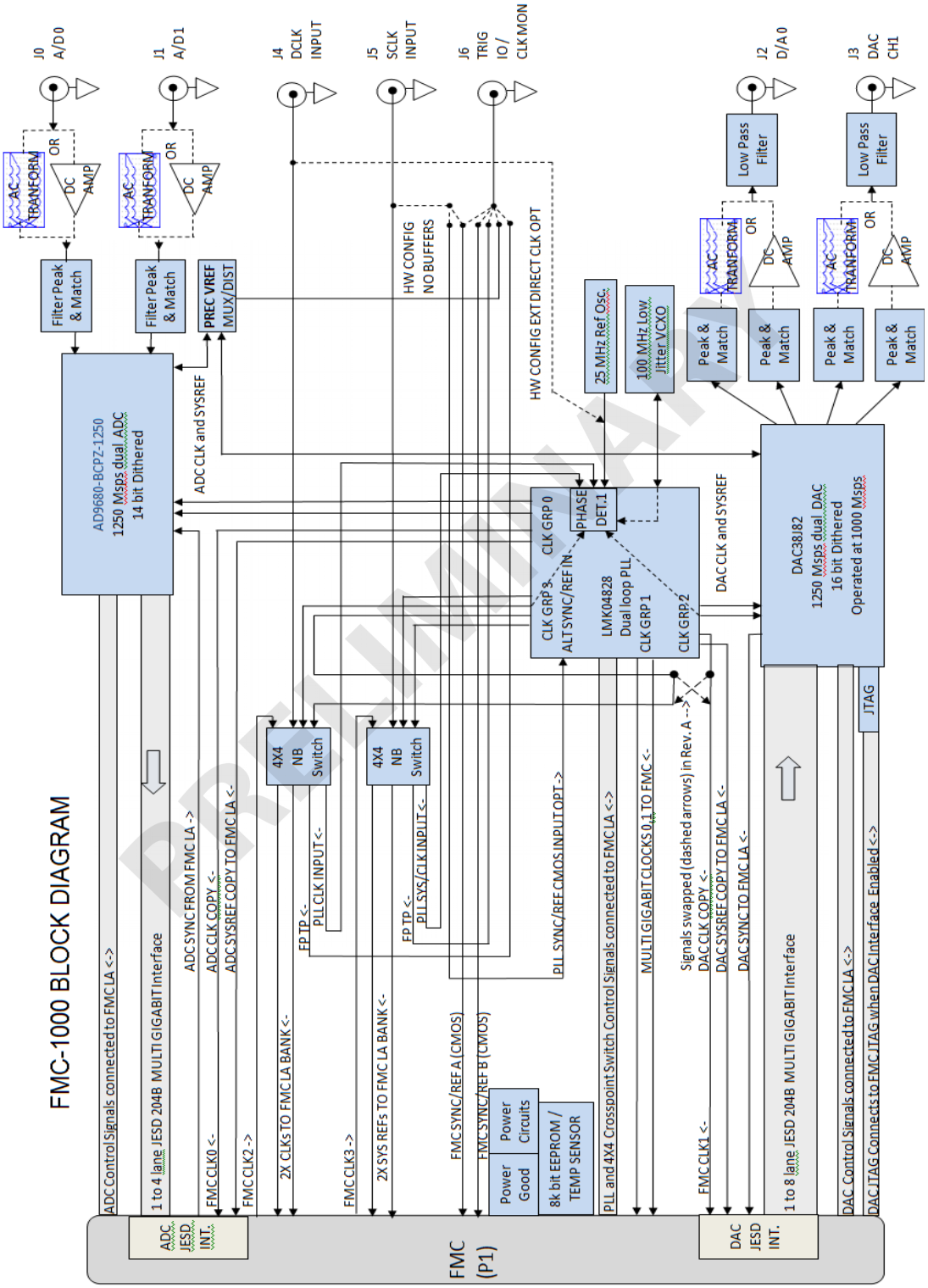
ORDERING INFORMATION

Product	Part No.	Description
FMC-1000	80325-1-<ER>	FMC module with two 1000 MSPS 14-bit A/D channels, two 1230 MSPS D/A channels, PLL and timing controls, AC- coupled A/D and D/As
FMC-1000	80325-2-<ER>	Like 80325-1 except A/Ds and D/As are DC-coupled
FMC-1000	80325-4-<ER>	FMC module with two 1250 MSPS 14-bit A/D channels, two 1230 MSPS D/As channel, PLL and timing controls, AC- coupled A/D and D/As
FMC-1000	80325-5-<ER>	Like 80325-4 except A/Ds and D/As are DC-coupled
Cables		
SSMC to BNC cable	67156	IO cable with SSMC (male) to BNC (male), 1 meter
Carrier Cards		
PEX6-COP	80284-x-<ER>	Desktop/server PCI Express FPGA co-processor card with FMC site
Embedded Computer Hosts		
ePC-K7	90502-x-<ER>	ePC-K7, I7 CPU, K325/410-T2 Commercial FPGA. Embedded PC with support for two FMC modules; i7 quad core COM Express Type 6 CPU; Windows/Linux drivers
Mini-K7	90600-x-<ER>	Mini-K7, I7 CPU, K325/410-T2 Commercial FPGA. Embedded PC with support for one FMC modules; Atom dual core COM Express Type 6 CPU; Windows/Linux drivers

<ER> corresponds to the Environmental Rating, L0...L4.

Physicals	
Form Factor	FMC VITA 57.1 single-width
Size	76.5 x 69 mm 10 mm mounting height
Weight	180g (approximate, contact factory if critical to application)
Hazardous Materials	Lead-free and RoHS compliant

FMC-1000



FMC-1000

Operating Environment Ratings

Modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

FMC-1000

Standard Features

Analog Inputs	
Inputs	2
Input Type	Single ended; AC or DC coupled
Nominal Input Impedance	50 ohm
A/D Device	Analog Devices AD9680BCPZ-1250 (AD9680BCPZ-1000 for 1000 Msps models)
Resolution	14-bit
f_{ADC}* Sample Rate	300 Msps to 1000 Msps/1250 Msps (each input, A/D IC data transfer rate is 2X)
Aperture Jitter	55 fs typical

Analog Outputs	
Outputs	2
Output Type	Single ended; AC or DC coupled
Nominal Output Impedance	50 ohm
D/A Device	Texas Instruments DAC38J82
Resolution	16-bit
f_{DAC}* Update Rate	100 to 1230 Msps (1x interpolation) 100 to 2460 Msps (2x interpolation) 100 to 2500 Msps (>=4x interpolation) (each output, D/A IC data transfer rate is 2X)
Interpolation	1x to 16x (11 clock cycle digital latency possible with no interpolation (1x), FIFO off, mixer off, QNC off, and inverse sinc off)

*Possible clock and sample rates in an application can depend on hardware configuration, carrier and system design

Clocks and Triggering	
Clock Sources*	LMK04828 dual loop PLL 1st loop 100 MHz TCVCXO standard 2nd loop 2 VCOs on chip VCO0 from 2370 to 2630 MHz VCO1 from 2920 to 3080 MHz 1000 MHz Jitter (VCO2 at 3GHz with Output Divider = 3 (1-32 allowed)) < 100 fs (10 kHz to 20 MHz) < 140 fs (100 Hz to 150 MHz)
	External (user supplied)
PLL Reference	External or 25MHz TCXO 25MHz ref is +/-250ppb -40to +85C (used for FMC-1000 test and specification)
PLL Resolution*	<12 kHz typical tuning resolution (depends on PLL configuration)
Triggering	Software: Continuous or acquire N frames External: DC coupled Logic Input
Channel Clocking	All channels can be synchronized to (TBD) clock cycles
Multi-card Synchronization	External triggering and clock inputs may be used for synchronization, and sync signals can be set through the FMC PLL SPI control interface.

Analog Channels Crosstalk between...	AC coupled A/Ds	< -52	dB	Measured on terminated victim channel, other 95% FS 30 MHz sine (preliminary, improvements likely)
	DC coupled A/Ds	< -90	dB	Measured on terminated victim channel, other 95% FS 30 MHz sine
	D/As	< -70	dB	Measured on terminated victim channel, other 95% FS 30 MHz sine
	A/D to/from D/A	< -90	dB	Measured on terminated victim channel, other 95% FS 30 MHz sine

Power		
All AC coupled	Total	10.4W
	3.3V	6.9W (2.1A)
	2.5V Vadj	3.5W (1.4A)
All DC coupled	Total	12W
	3.3V	8.2W (2.5A)
	2.5V Vadj	3.8W (1.52A)
Heat Sinking		Conduction cooling supported, system level thermal design may be required

A/D ELECTRICAL CHARACTERISTICS

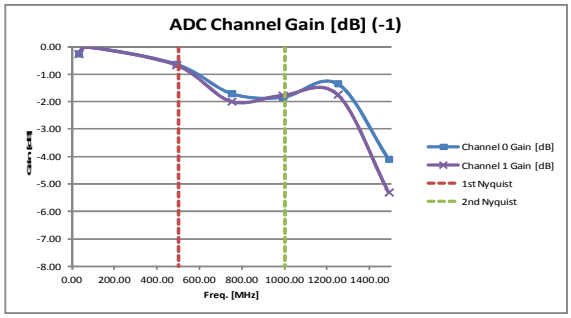
Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter		Typ	Units	Notes
A/D Channels				
Bandwidth		10, 1300	MHz	-3dB, AC coupled inputs
		500	MHz	-3dB, DC coupled inputs
Flatness		+/-0.4	dB	50 to 500 MHz, AC Coupled
		+/-1.5	dB	0 to 500 MHz, DC Coupled
Range	AC Coupled	2	Vpp	Nominal
		10	dBm	Nominal in a 50 Ohm system
		2.6	Vpp	Absolute maximum (to avoid damage)
		+/-10	V	DC withstanding from 0V
	DC Coupled	+/-0.42	V	Nominal from 0V
		1.5	dBm	Nominal in a 50 Ohm system
		+/-1	V	Absolute maximum from 0V (to avoid damage)
SNR		65.4, 60.1	dB(typ)	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		63.2, 59.5	dB(typ)	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		61.5, 56.0	dB(typ)	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
ENOB		10.8, 9.9	bits(typ)	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC, DC Coupled
		10.7, 9.5	bits(typ)	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		10.5, 8.8	bits(typ)	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
SFDR		84.1, 82.7	dB(typ)	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		82.3, 65	dB(typ)	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		78, 60	dB(typ)	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
THD		-75, -80	dBc(typ)	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		-75, -75	dBc(typ)	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		-72, -58	dBc(typ)	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
NSD		-152.7, -147.6	dBFS/Hz	F = 70.1 MHz; AC,DC Coupled
		-150.0, -145.5	dBFS/Hz	F = 141.1 MHz; AC,DC Coupled
		-148.9, -142.0	dBFS/Hz	F = 252.85 MHz; AC,DC Coupled
Offset Error (absolute value maximum)		1	mV	Factory calibration, average of 64K samples after warmup.
Gain Error (absolute value maximum)		0.5	%	Factory calibration after warmup.

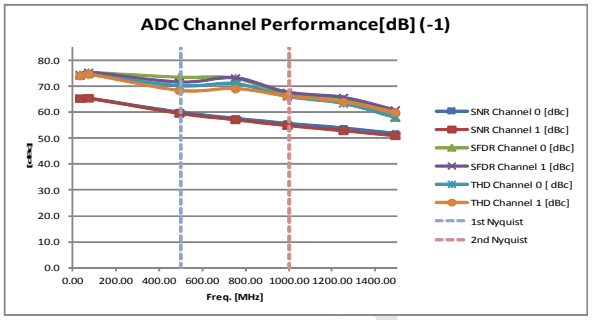
D/A ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, f_{DAC} =2 Gsps, 95%FS, 2X interpolation,PLL enabled unless otherwise noted.

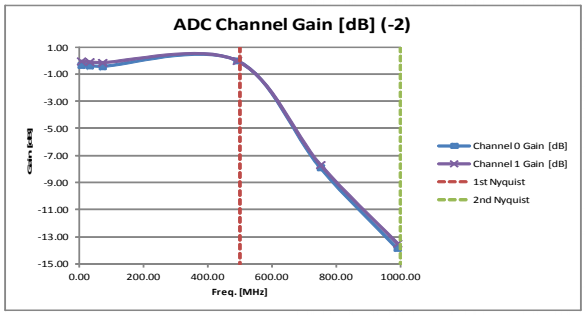
Parameter		Typical	Units	Notes
DAC Channels				
Bandwidth (Note 1)		10, 1000	MHz	Typical, AC Coupled
		600	MHz	Typical, DC Coupled
Output Amplitude Variation (Note 1)		+/-0.4	dB	10-500 MHz, AC Coupled
		+/-0.5	dB	0-300 MHz, DC Coupled (from a best fit line with gain slope of approximately 0.4dB/100MHz)
Range	AC Coupled	0.9	Vpp	Nominal
		2	dBm	Nominal in a 50 Ohm system
		+/-10	V	DC withstanding from 0V
	DC Coupled	+/- 0.5	V	Nominal from 0V
		2.5	dBm	Nominal in a 50 Ohm system
SNR (Note 2)		72.5, 68	dB	Fout = 70.1 MHz, 95% FS sine; AC,DC Coupled
		70, TBD	dB	Fout = 141.1 MHz, 95% FS sine; AC,DC Coupled
		64, TBD	dB	Fout = 252.85 MHz, 95% FS sine; AC,DC Coupled
SFDR (Note 3)		77, 55	dB	Fout = 70.1 MHz, 95% FS sine; AC,DC Coupled
		71, TBD	dB	Fout = 141.1 MHz, 95% FS sine; AC,DC Coupled
		66, TBD	dB	Fout = 252.85 MHz, 95% FS sine; AC,DC Coupled
THD (Note 3)		-73, -46	dBc	Fout = 70.1 MHz, 95% FS sine; AC,DC Coupled
		-70, -33	dBc	Fout = 141.1 MHz, 95% FS sine; AC,DC Coupled
		-62, -25	dBc	Fout = 252.85 MHz, 95% FS sine; AC,DC Coupled
NSD***		-160.5, -155	dBFS/Hz	F = 70.1 MHz; AC,DC Coupled
		-158.6, TBD	dBFS/Hz	F = 141.1 MHz; AC,DC Coupled
		-155.5, TBD	dBFS/Hz	F = 252.85 MHz; AC,DC Coupled
Gain Error (absolute value maximum)		0.5	% of FS	Calibrated
Offset Error (absolute value maximum)		1	mV	Calibrated



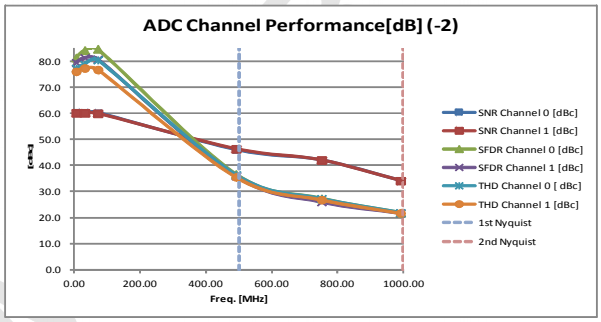
(a) ADC normalized gain vs. frequency (AC version)



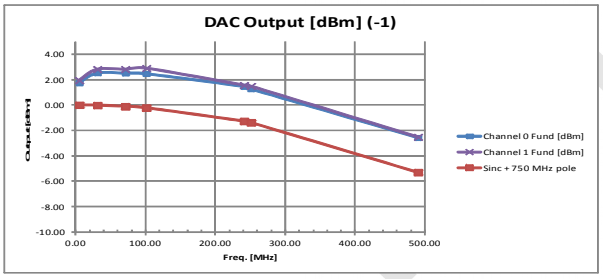
(b) ADC SNR/SFDR/THD vs frequency (AC version)



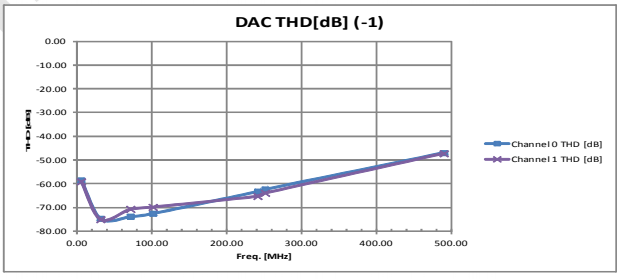
(c) ADC normalized gain vs frequency (DC version)



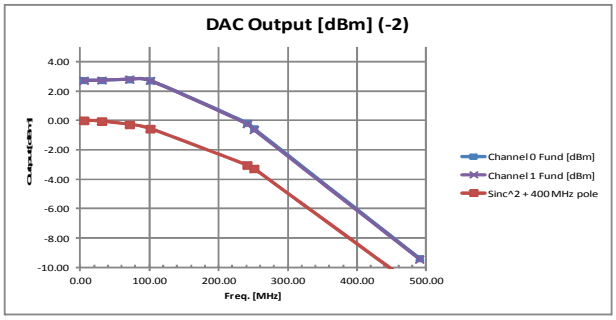
(d) ADC SNR/SFDR/THD vs frequency (DC version)



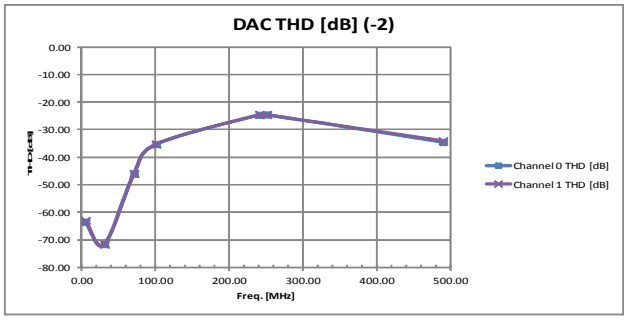
(e) DAC normalized gain vs frequency (AC version)



(f) DAC THD vs frequency (AC version)



(g) DAC normalized gain vs frequency (DC version)



(h) DAC THD vs frequency (DC version)

Fig. 1 Representative performance plots for the ADC and DAC.

Notes:

1. First, it is important to note that for the DAC, any attempt to convey an output signal in the 2nd Nyquist zone ($0.5\ f_{clk} < f_{out} < f_{clk}$) will result in output an output signal indistinguishable from its 1st Nyquist zone image. For example, a 750 MHz sine wave (absent any signal processing) clocked at 1000 MHz and a 250 MHz sine wave would be identical by any external measurement. Thus conveying a 2nd Nyquist zone signal requires the use of a suitable highpass or bandpass filter. For the 750 MHz example just introduced, a filter that passes 750 MHz and strongly rejects the 250 MHz image (which would be stronger than the desired output) is required. That being said, the raw output of the DAC would be "colored" by the response of the circuitry between the DAC IC and the output connector. This lowpass response for the -1 (AC) version follows a $\text{sinc}(\pi\ f_{out}/f_{clk})$ + 750 MHz pole response. For the -2 (DC) version it follows a $[\text{sinc}(\pi\ f_{out}/f_{clk})]^2$ + 400 MHz pole response. These responses are plotted out in Fig. 1(e) and Fig. 1(g) on page 9 of this datasheet.

3. THD was measured directly using a spectrum analyzer. For practicality, only the second and third harmonics were used in the calculation (as the fourth and higher order harmonics were small enough not to affect the computed value for the frequencies at which these data were taken). See Fig. 1(f) and Fig. 1(h) for representative plots of THD.

FMC-1000 analog performance is specified like the D/A IC is specified, with a 20 mA full scale output. The FMC-1000 maximum output range is specified at (and the hardware is configured for) approximately 30 mA full scale, the maximum full scale amplitude of the D/A IC. The D/A full scale output current can be set in 1/16 increments of the maximum using the D/A IC's 4 bit coarse gain control. This allows a setting of 20.625 mA which is less than 3.2% larger than 20 mA. This difference (0.26dB) is not significant for analog specification purposes. However the output range will be scaled proportionally (11/16 of specified) when this is done.

500 MHz BW was used for DAC SNR.

The preliminary FMC-1000 analog performance is based on prototypes using the 1000Msps A/D IC. At the time of writing the 1000 Msps part has better specified analog performance at 1000 Msps, but the 1250 Msps A/D IC is being revised by the vendor (final analog performance TBD at IC release). For preliminary FMC-1000 performance estimates at 1000 Msps the difference between 1000 and 1250 Msps ICs is TBD, and too small to be estimated accurately at the current time. So preliminary performance numbers apply to both versions, but are more preliminary for FMC-1000 models using the 1250 Msps capable A/D IC.

Gain Definition

FMC-1000 is specified and tested with a 50 Ohm source impedance (unless otherwise noted). The FMC-1000 nominal gain is approximately 1X or 0dB when calibrated, the voltage at the FMC-1000 input equals the digital reading output. The internal hardware (raw) gain of the FMC-1000 may be different, for example when DC coupled the A/D IC sees about twice the voltage applied at the FMC-1000 input.

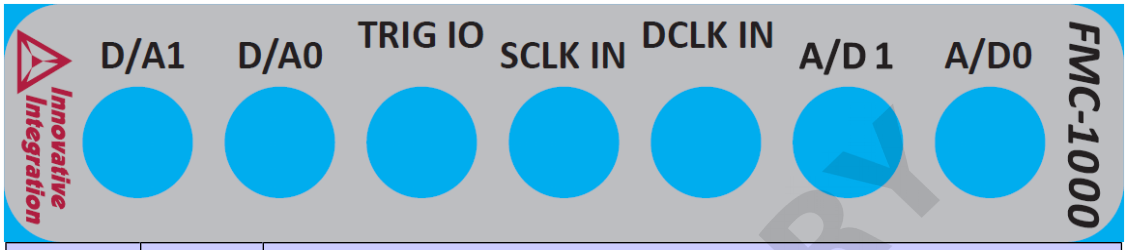
Variations in source impedance change the system gain. The 50 Ohm terminations in a RF system are rarely physical resistors (they are the Thévenin equivalent of the circuit). At lower input frequencies 50 Ohm source terminations are not common but are needed for continuity with higher frequency 50 Ohm measurements. This source 50 Ohm series termination forms a voltage divider with the FMC-1000 input impedance reducing the source voltage by approximately ½ at the FMC-1000 input. Replacing it with a series 0 Ohm source resistance will change the system gain about 2X in Voltage or 6 dB.

Digital Calibration Note

The FMC-1000 can be digitally calibrated for offset and gain. However if the signal is clipped (outside the A/D range) the information is lost, so the raw gain is typically designed for a signal level at the A/D that is slightly less than A/D Full Scale in the bandwidth of interest to allow the nominal input range to be measured accurately without clipping when digitally calibrated.

FMC-1000

Front Panel (Bezel) Detail



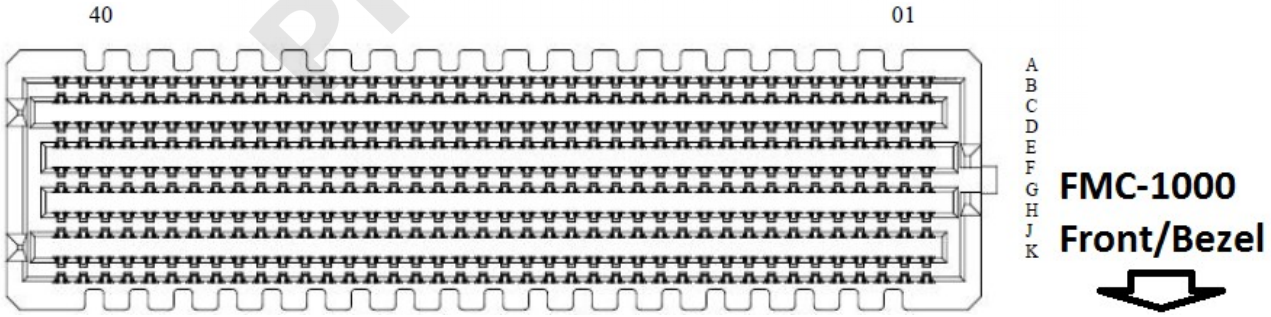
Front Panel Label	Schematic reference	Description
A/D 0	J0	A/D analog input 50 Ohm nominal impedance AC or DC coupled by model
A/D 1	J1	A/D analog input 50 Ohm nominal impedance AC or DC coupled by model
DCLK IN	J4	Logic input, 1.25V +/- 0.1V threshold, nominal range 0V to 2.5V, high impedance, DC coupled with an approximately10 kOhm pull down in standard configuration. Can be hardware configured for different threshold voltages from 0.15 to 2.35V, as AC or DC coupled, with or without a termination. The standard hardware configuration connects this to a 4X4 non-blocking cross-point switch allowing multiple uses as a clock reference or trigger routed to the FMC-1000 PLL and the carrier. Also this input can be hardware configured as direct PLL clock input (CLKin1) which can be used as a PLL input/reference or simply distributed (no PLL) for use as the FMC-1000 sampling clock.
SCLK IN	J5	Logic input, 1.25V +/- 0.1V threshold, nominal range 0V to 2.5V, high impedance, DC coupled with an approximately 10 kOhm pull down in standard configuration. Can be hardware configured for different threshold voltages from 0.15 to 2.35V, as AC or DC coupled with or without a termination. The standard hardware configuration connects this to a 4X4 non-blocking cross-point switch allowing multiple uses as a clock or trigger routed to the FMC-1000 PLL and the carrier. When connected to the PLL input (SYNCIn0/CLKin0) it can also be used for cyclical sync or clock signals. This pin can be hardware configured for bidirectional connection to the FMC carrier interface (2.5V LVCMOS). Also this input can be hardware configured for direct PLL “single shot” sync signals (PLL SYNC PIN 6 supports basic “single shot” sync in addition to higher level PLL modes, like triggering a controlled number of SYSREF pulses). PLL pin 6 should not be used for cyclical signals as it can AC crosstalk to the PLL outputs (instead use SYNCIn0/CLKin0 for cyclical signals)
TRIG IO	J6	Hardware Configurable IO, Standard configuration; sampling clock monitor output 0.4V to 1.65 Vpp into 50 Ohms, with weak DC bias from Vref (1V nominal) see block diagram for possible hardware configurations
D/A 0	J2	D/A analog output 50 Ohm nominal impedance AC or DC coupled by model
D/A 1	J3	D/A analog output 50 Ohm nominal impedance AC or DC coupled by model
ALL	ALL	*ENTERTEC 13460334 SSMC JACK RIGHT ANGLE EXTENDED BARREL*

Note: 2.5 V logic inputs absolute maximum 2.8V, absolute minimum -0.3V

FMC-1000

FMC Interface Detail	
IO	LA[33:0] pairs, HA[23:0] pairs & HB[21:0] pairs (un-driven pins grounded for improved signal integrity) DP[0..7]_C2M_N,P (JESD 204B subclass 1 DAC data lanes up to 12.5 Gbps each*) DP[0..3]_M2C_N,P (JESD 204B subclass 1 ADC data lanes up to 12.5 Gbps each*)
IO Standards	FMC DP: JESD204B (subclass 1) FMC LA, HA and HB: Differential: LVDS Single Ended: 2.5V LVCMOS FMC Control Signals: 3.3V LVTTL FMC Clocks (bidirectional clocks driven by carrier): LVDS
Required voltages	FMC 3P3V and 3P3VAUX = 3.3V +/- 4% FMC VADJ = 2.5V +/- 4% To reduce FMC-1000 power consumption, FMC Voltages are used without re-regulation and are specified at +/- 4% (this is not usually a issue as FMC-1000 maximum supply currents are smaller than the FMC maximums), the FMC-1000 can function with wider Voltage tolerance but is specified with +/-4% Voltage supplies. FMC 12P0V (12V) is not used in standard FMC-1000 hardware configurations, it is routed to a wire terminal / test point on the FMC-1000 for optional system / customer use.

FMC Connector Grid (Component side)



FMC-1000

FMC Connector Pins from VITA 57.1

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

FMC-1000

FMC-1000 FMC Connector Signals Detail.... Bank A

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
A1	GND	GND	**ADC JESD 204B DATA**
A2	DP1_M2C_P	ADC_TX1_TO_FMC_DP1_M2C_P	AC Coupled, set A/D IC output to swap P/N
A3	DP1_M2C_N	ADC_TX1_TO_FMC_DP1_M2C_N	AC Coupled, set A/D IC output to swap P/N
A4	GND	GND	
A5	GND	GND	
A6	DP2_M2C_P	ADC_TX2_TO_FMC_DP2_M2C_P	AC Coupled, set A/D IC output to swap P/N
A7	DP2_M2C_N	ADC_TX2_TO_FMC_DP2_M2C_N	AC Coupled, set A/D IC output to swap P/N
A8	GND	GND	
A9	GND	GND	
A10	DP3_M2C_P	ADC_TX3_TO_FMC_DP3_M2C_P	AC Coupled, set A/D IC output to swap P/N
A11	DP3_M2C_N	ADC_TX3_TO_FMC_DP3_M2C_N	AC Coupled, set A/D IC output to swap P/N
A12	GND	GND	
A13	GND	GND	
A14	DP4_M2C_P	no connection	
A15	DP4_M2C_N	no connection	
A16	GND	GND	
A17	GND	GND	
A18	DP5_M2C_P	no connection	
A19	DP5_M2C_N	no connection	
A20	GND	GND	
A21	GND	GND	**DAC JESD 204B DATA**
A22	DP1_C2M_P	DAC_RX6_TO_FMC_DP1_C2M_P	AC Coupled, set D/A IC output to swap P/N
A23	DP1_C2M_N	DAC_RX6_TO_FMC_DP1_C2M_N	AC Coupled, set D/A IC output to swap P/N
A24	GND	GND	
A25	GND	GND	
A26	DP2_C2M_P	DAC_RX5_TO_FMC_DP2_C2M_P	AC Coupled
A27	DP2_C2M_N	DAC_RX5_TO_FMC_DP2_C2M_N	AC Coupled
A28	GND	GND	
A29	GND	GND	
A30	DP3_C2M_P	DAC_RX4_TO_FMC_DP3_C2M_P	AC Coupled, set D/A IC output to swap P/N
A31	DP3_C2M_N	DAC_RX4_TO_FMC_DP3_C2M_N	AC Coupled, set D/A IC output to swap P/N
A32	GND	GND	
A33	GND	GND	
A34	DP4_C2M_P	DAC_RX3_TO_FMC_DP4_C2M_P	AC Coupled, set D/A IC output to swap P/N
A35	DP4_C2M_N	DAC_RX3_TO_FMC_DP4_C2M_N	AC Coupled, set D/A IC output to swap P/N
A36	GND	GND	
A37	GND	GND	
A38	DP5_C2M_P	DAC_RX2_TO_FMC_DP5_C2M_P	AC Coupled
A39	DP5_C2M_N	DAC_RX2_TO_FMC_DP5_C2M_N	AC Coupled
A40	GND	GND	

FMC-1000

Bank B

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
B1	CLK_DIR	P_3V3_AUX	3.3V, 10K Ohm pull up to P_3V3_AUX, bidirectional clocks are C2M
B2	GND	GND	
B3	GND	GND	
B4	DP9_M2C_P	no connection	
B5	DP9_M2C_N	no connection	
B6	GND	GND	
B7	GND	GND	
B8	DP8_M2C_P	no connection	
B9	DP8_M2C_N	no connection	
B10	GND	GND	
B11	GND	GND	
B12	DP7_M2C_P	no connection	
B13	DP7_M2C_N	no connection	
B14	GND	GND	
B15	GND	GND	
B16	DP6_M2C_P	no connection	
B17	DP6_M2C_N	no connection	
B18	GND	GND	
B19	GND	GND	
B20	GBTCLK1_M2C_P	GBTCLK1_P	LVDS
B21	GBTCLK1_M2C_N	GBTCLK1_N	LVDS
B22	GND	GND	
B23	GND	GND	
B24	DP9_C2M_P	no connection	
B25	DP9_C2M_N	no connection	
B26	GND	GND	
B27	GND	GND	
B28	DP8_C2M_P	no connection	
B29	DP8_C2M_N	no connection	
B30	GND	GND	
B31	GND	GND	**DAC JESD 204B DATA**
B32	DP7_C2M_P	DAC_RX0_TO_FMC_DP7_C2M_P	AC Coupled
B33	DP7_C2M_N	DAC_RX0_TO_FMC_DP6_C2M_N	AC Coupled
B34	GND	GND	
B35	GND	GND	
B36	DP6_C2M_P	DAC_RX1_TO_FMC_DP6_C2M_P	AC Coupled, set D/A IC output to swap P/N
B37	DP6_C2M_N	DAC_RX1_TO_FMC_DP6_C2M_N	AC Coupled, set D/A IC output to swap P/N
B38	GND	GND	
B39	GND	GND	
B40	RES0	no connection	

FMC-1000

Bank C

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
C1	GND	GND	**DAC JESD 204B DATA**
C2	DP0_C2M_P	DP0_C2M_P	AC Coupled: DAC_RX6_TO_FMC_DP0_C2M_P
C3	DP0_C2M_N	DP0_C2M_N	AC Coupled: DAC_RX6_TO_FMC_DP0_C2M_N
C4	GND	GND	
C5	GND	GND	**ADC JESD 204B DATA**
C6	DP0_M2C_P	DP0_M2C_P	AC Coupled, set A/D IC output to swap P/N: ADC_TX0_TO_FMC_DP0_M2C
C7	DP0_M2C_N	DP0_M2C_N	AC Coupled, set A/D IC output to swap P/N: ADC_TX0_TO_FMC_DP0_M2C
C8	GND	GND	
C9	GND	GND	
C10	LA06_P	FMC_LA6_TP	TP33 with 10K pull down to ground
C11	LA06_N	ADC_PDWN/STBY	No Connection in standard product
C12	GND	GND	
C13	GND	GND	
C14	LA10_P	ADC_SCLK	Due to capacitive loading and unknown driver (carrier) strength, interface clocks >2 MHz should be tested
C15	LA10_N	ADC_CSB	
C16	GND	GND	
C17	GND	GND	
C18	LA14_P	CLK_MUX_SI/SEL1	
C19	LA14_N	SY_MUX_SEL0	
C20	GND	GND	
C21	GND	GND	
C22	LA18_P_CC	FMC_CLK_4X4_OUT1_P	LVDS
C23	LA18_N_CC	FMC_CLK_4X4_OUT1_N	LVDS
C24	GND	GND	
C25	GND	GND	
C26	LA27_P	DAC_SDO	
C27	LA27_N	DAC_SDIO_DIR	
C28	GND	GND	
C29	GND	GND	
C30	SCL	FMC_SCL	3.3V, 10K Ohm PU, Due to capacitive loading and unknown driver (carrier) strength, interface clocks >2 MHz should be tested
C31	SDA	FMC_SDA	3.3V, 10K Ohm PU (pull up)
C32	GND	GND	
C33	GND	GND	
C34	GA0	FMC_GA0	3.3V
C35	12P0V	P_12V0	Not used on standard model, connected to through hole test point (TP36) for potential external use
C36	GND	GND	
C37	12P0V	P_12V0	Not used on standard model, connected to through hole test point (TP36) for potential external use
C38	GND	GND	
C39	3P3V	P_3V3_FMC	
C40	GND	GND	

FMC-1000

Bank D

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
D1	PG_C2M	FMC_PG_C2M	3.3V
D2	GND	GND	
D3	GND	GND	
D4	GBTCLK0_M2C_P	GBTCLK0_P	LVDS
D5	GBTCLK0_M2C_N	GBTCLK0_N	LVDS
D6	GND	GND	
D7	GND	GND	
D8	LA01_P_CC	FMC_SYS_4X4_OUT1_P	LVDS
D9	LA01_N_CC	FMC_SYS_4X4_OUT1_N	LVDS
D10	GND	GND	
D11	LA05_P	FMC_SYNC/REF_B	
D12	LA05_N	FMC_SYNC/REF_A	
D13	GND	GND	
D14	LA09_P	ADC_SDI	
D15	LA09_N	ADC_SDO	
D16	GND	GND	
D17	LA13_P	CLK_MUX_SEL0	
D18	LA13_N	CLK_MUX_SCLK	
D19	GND	GND	
D20	LA17_P_CC	FMC_CLK_4X4_OUT0_P	LVDS
D21	LA17_N_CC	FMC_CLK_4X4_OUT0_N	LVDS
D22	GND	GND	
D23	LA23_P	PLL_SDI	
D24	LA23_N	PLL_SDO	
D25	GND	GND	
D26	LA26_P	DAC_SD_EN _N	
D27	LA26_N	DAC_SDIO	
D28	GND	GND	
D29	TCK	DAC_TCLK	3.3V
D30	TDI	DAC_TDI	3.3V
D31	TDO	DAC_TDO	3.3V
D32	3P3VAUX	P_3V3_AUX	
D33	TMS	DAC_TMS	3.3V
D34	TRST_L	DAC_TRST_N	3.3V
D35	GA1	FMC_GA1	3.3V
D36	3P3V	P_3V3_FMC	
D37	GND	GND	
D38	3P3V	P_3V3_FMC	
D39	GND	GND	
D40	3P3V	P_3V3_FMC	

FMC-1000

Bank E

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
E1	GND	GND	
E2	HA01_P_CC	GND	
E3	HA01_N_CC	GND	
E4	GND	GND	
E5	GND	GND	
E6	HA05_P	GND	
E7	HA05_N	GND	
E8	GND	GND	
E9	HA09_P	GND	
E10	HA09_N	GND	
E11	GND	GND	
E12	HA13_P	GND	
E13	HA13_N	GND	
E14	GND	GND	
E15	HA16_P	GND	
E16	HA16_N	GND	
E17	GND	GND	
E18	HA20_P	GND	
E19	HA20_N	GND	
E20	GND	GND	
E21	HB03_P	GND	
E22	HB03_N	GND	
E23	GND	GND	
E24	HB05_P	GND	
E25	HB05_N	GND	
E26	GND	GND	
E27	HB09_P	GND	
E28	HB09_N	GND	
E29	GND	GND	
E30	HB13_P	GND	
E31	HB13_N	GND	
E32	GND	GND	
E33	HB19_P	GND	
E34	HB19_N	GND	
E35	GND	GND	
E36	HB21_P	GND	
E37	HB21_N	GND	
E38	GND	GND	
E39	VADJ	P_2V5_FMC	
E40	GND	GND	

FMC-1000

Bank F

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
F1	PG_M2C	FMC_PG_M2C	3.3V, open drain output with 577 Ohm pull up to P_3V3_AUX
F2	GND	GND	
F3	GND	GND	
F4	HA00_P_CC	GND	
F5	HA00_N_CC	GND	
F6	GND	GND	
F7	HA04_P	GND	
F8	HA04_N	GND	
F9	GND	GND	
F10	HA08_P	GND	
F11	HA08_N	GND	
F12	GND	GND	
F13	HA12_P	GND	
F14	HA12_N	GND	
F15	GND	GND	
F16	HA15_P	GND	
F17	HA15_N	GND	
F18	GND	GND	
F19	HA19_P	GND	
F20	HA19_N	GND	
F21	GND	GND	
F22	HB02_P	GND	
F23	HB02_N	GND	
F24	GND	GND	
F25	HB04_P	GND	
F26	HB04_N	GND	
F27	GND	GND	
F28	HB08_P	GND	
F29	HB08_N	GND	
F30	GND	GND	
F31	HB12_P	GND	
F32	HB12_N	GND	
F33	GND	GND	
F34	HB16_P	GND	
F35	HB16_N	GND	
F36	GND	GND	
F37	HB20_P	GND	
F38	HB20_N	GND	
F39	GND	GND	
F40	VADJ	P_2V5_FMC	

FMC-1000

Bank G

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
G1	GND	GND	
G2	CLK1_M2C_P	Rev B and above: DAC_CLK_P	Rev A: ADC_SYS_P, All revs LVDS
G3	CLK1_M2C_N	Rev B and above: DAC_CLK_N	Rev A: ADC_SYS_N, All revs LVDS
G4	GND	GND	
G5	GND	GND	
G6	LA00_P_CC	FMC_SYS_4X4_OUT0_P	LVDS
G7	LA00_N_CC	FMC_SYS_4X4_OUT0_N	LVDS
G8	GND	GND	
G9	LA03_P	DAC_SYN_P	LVDS
G10	LA03_N	DAC_SYN_N	LVDS
G11	GND	GND	
G12	LA08_P	ADC_FD_0	
G13	LA08_N	ADC_FD_1	
G14	GND	GND	
G15	LA12_P	CLK_MUX_MODE	
G16	LA12_N	CLK_MUX_LOAD	
G17	GND	GND	
G18	LA16_P	PLL_RESET	
G19	LA16_N	PLL_GPO	
G20	GND	GND	
G21	LA20_P	PLL_UTIL_3	
G22	LA20_N	PLL_UTIL_4	
G23	GND	GND	
G24	LA22_P	PLL_CS_N	
G25	LA22_N	PLL_SCK	Due to capacitive loading and unknown driver (carrier) strength, interface clocks >2 MHz should be tested
G26	GND	GND	
G27	LA25_P	DAC_SLEEP	
G28	LA25_N	DAC_SCLK	
G29	GND	GND	
G30	LA29_P	DAC_ALARM	
G31	LA29_N	FMC_SYSTEM_LED	Not connected in standard model
G32	GND	GND	
G33	LA31_P	FMC_ADC_READY_N	Not connected in standard model
G34	LA31_N	FMC_DAC_READY_N	Not connected in standard model
G35	GND	GND	
G36	LA33_P	UTILITY_JP2_2	connected to JP2 utility connector pin 2 (JP2 not populated in standard product)
G37	LA33_N	UTILITY_JP2_4	connected to JP2 utility connector pin 4 (JP2 not populated in standard product)
G38	GND	GND	
G39	VADJ	P_2V5_FMC	
G40	GND	GND	

FMC-1000

Bank H

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
H1	VREF_A_M2C	no connection	
H2	PRSNT_M2C_L	GND	
H3	GND	GND	
H4	CLK0_M2C_P	ADC_CLK_P	LVDS
H5	CLK0_M2C_N	ADC_CLK_N	LVDS
H6	GND	GND	
H7	LA02_P	DAC_SYS_P	LVDS
H8	LA02_N	DAC_SYS_N	LVDS
H9	GND	GND	
H10	LA04_P	ADC_SYN_P	LVDS
H11	LA04_N	ADC_SYN_N	LVDS
H12	GND	GND	
H13	LA07_P	Rev B and above: ADC_SYS_P	Rev A: DAC_CLK_P, All revs LVDS
H14	LA07_N	Rev B and above: ADC_SYS_N	Rev A: DAC_CLK_N, All revs LVDS
H15	GND	GND	
H16	LA11_P	SY_MUX_MODE	
H17	LA11_N	SY_MUX_LOAD	
H18	GND	GND	
H19	LA15_P	SY_MUX_SCLK	
H20	LA15_N	SY_MUX_SI/SEL1	
H21	GND	GND	
H22	LA19_P	PLL_UTIL_1	
H23	LA19_N	PLL_UTIL_2	
H24	GND	GND	
H25	LA21_P	PLL_UTIL_3_DIR	
H26	LA21_N	PLL_UTIL_4_DIR	
H27	GND	GND	
H28	LA24_P	DAC_RESET_N	
H29	LA24_N	DAC_TX_EN	
H30	GND	GND	
H31	LA28_P	DAC_SYNC_AB_N	
H32	LA28_N	DAC_SYNC_CD_N	
H33	GND	GND	
H34	LA30_P	FMC_USER_DEF_POW_EN	Not connected in standard model
H35	LA30_N	FMC_USER_DEF_POW_PG	Not connected in standard model
H36	GND	GND	
H37	LA32_P	FMC_PG_M2C_ALT	Not connected in standard model
H38	LA32_N	FMC_TEMP_ALRT	Also connected to JP2 utility connector pin 6 (JP2 not populated in standard product)
H39	GND	GND	
H40	VADJ	P_2V5_FMC	

FMC-1000

Bank J

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
J1	GND	GND	
J2	CLK3_BIDIR_P	FMC_CLK3_P	LVDS
J3	CLK3_BIDIR_N	FMC_CLK3_N	LVDS
J4	GND	GND	
J5	GND	GND	
J6	HA03_P	GND	
J7	HA03_N	GND	
J8	GND	GND	
J9	HA07_P	GND	
J10	HA07_N	GND	
J11	GND	GND	
J12	HA11_P	GND	
J13	HA11_N	GND	
J14	GND	GND	
J15	HA14_P	GND	
J16	HA14_N	GND	
J17	GND	GND	
J18	HA18_P	GND	
J19	HA18_N	GND	
J20	GND	GND	
J21	HA22_P	GND	
J22	HA22_N	GND	
J23	GND	GND	
J24	HB01_P	GND	
J25	HB01_N	GND	
J26	GND	GND	
J27	HB07_P	GND	
J28	HB07_N	GND	
J29	GND	GND	
J30	HB11_P	GND	
J31	HB11_N	GND	
J32	GND	GND	
J33	HB15_P	GND	
J34	HB15_N	GND	
J35	GND	GND	
J36	HB18_P	GND	
J37	HB18_N	GND	
J38	GND	GND	
J39	VIO_B_M2C	P_VIO_B	2.5V (filtered VADJ)
J40	GND	GND	

FMC-1000

Bank K

P1 Pin	P1 Pin Name	FMC-1000 Net	NOTE:
K1	VREF_B_M2C	no connection	
K2	GND	GND	
K3	GND	GND	
K4	CLK2_BIDIR_P	FMC_CLK2_P	LVDS
K5	CLK2_BIDIR_N	FMC_CLK2_N	LVDS
K6	GND	GND	
K7	HA02_P	GND	
K8	HA02_N	GND	
K9	GND	GND	
K10	HA06_P	GND	
K11	HA06_N	GND	
K12	GND	GND	
K13	HA10_P	GND	
K14	HA10_N	GND	
K15	GND	GND	
K16	HA17_P_CC	GND	
K17	HA17_N_CC	GND	
K18	GND	GND	
K19	HA21_P	GND	
K20	HA21_N	GND	
K21	GND	GND	
K22	HA23_P	GND	
K23	HA23_N	GND	
K24	GND	GND	
K25	HB00_P_CC	GND	
K26	HB00_N_CC	GND	
K27	GND	GND	
K28	HB06_P_CC	GND	
K29	HB06_N_CC	GND	
K30	GND	GND	
K31	HB10_P	GND	
K32	HB10_N	GND	
K33	GND	GND	
K34	HB14_P	GND	
K35	HB14_N	GND	
K36	GND	GND	
K37	HB17_P_CC	GND	
K38	HB17_N_CC	GND	
K39	GND	GND	
K40	VIO_B_M2C	P_VIO_B	2.5V (filtered VADJ)

FMC-1000

IMPORTANT NOTICES

Innovative Integration Incorporated reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Innovative Integration's terms and conditions of sale supplied at the time of order acknowledgment.

Innovative Integration warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with Innovative Integration's standard warranty. Testing and other quality control techniques are used to the extent Innovative Integration deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Innovative Integration assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using Innovative Integration products. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Innovative Integration does not warrant or represent that any license, either express or implied, is granted under any Innovative Integration patent right, copyright, mask work right, or other Innovative Integration intellectual property right relating to any combination, machine, or process in which Innovative Integration products or services are used. Information published by Innovative Integration regarding third-party products or services does not constitute a license from Innovative Integration to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Innovative Integration under the patents or other intellectual property of Innovative Integration.

Reproduction of information in Innovative Integration data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice.

Innovative Integration is not responsible or liable for such altered documentation. Resale of Innovative Integration products or services with statements different from or beyond the parameters stated by Innovative Integration for that product or service voids all express and any implied warranties for the associated Innovative Integration product or service and is an unfair and deceptive business practice. Innovative Integration is not responsible or liable for any such statements.

For further information on Innovative Integration products and support see our web site:

www.innovative-dsp.com

Mailing Address: Innovative Integration, Inc.

741 Flynn Road, Camarillo, California 93012